Switched-Current Circuits

Synthesis and Analysis Techniques

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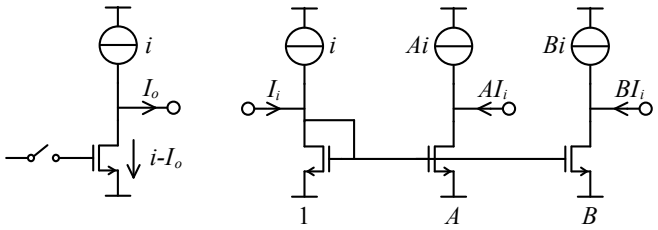
Outline:

- Introduction.
- First-generation SI delays and integrators.
- Second-generation SI cells
- Filter synthesis by the simulation of passive prototypes using bilinear integrators.
- Filter synthesis using Euler integrators.
- Component simulation technique.
- Imperfections and compensation techniques.
- Analysis methods.

Basic Principles

- Switched-current circuits implement discrete-time linear systems, using MOS transistors with the gate open as current memory elements..
- The memory elements are coupled by current mirrors.
- A clock system with two or more phases allows the connection of these basic elements to form delays, discrete-time integrators and filters.
- Current transfer functions are linear, even in large-signal operation.
- Linear capacitors and transconductors are not required. Precision depends on transistor matching.
- In the simplest form, single transistors are used as transconductors, current sources, and switches.
- This basic form is not sufficient for complex filters, due to errors introduced by G_{ds} conductances, C_{gd} capacitances, and clock feedthrough.



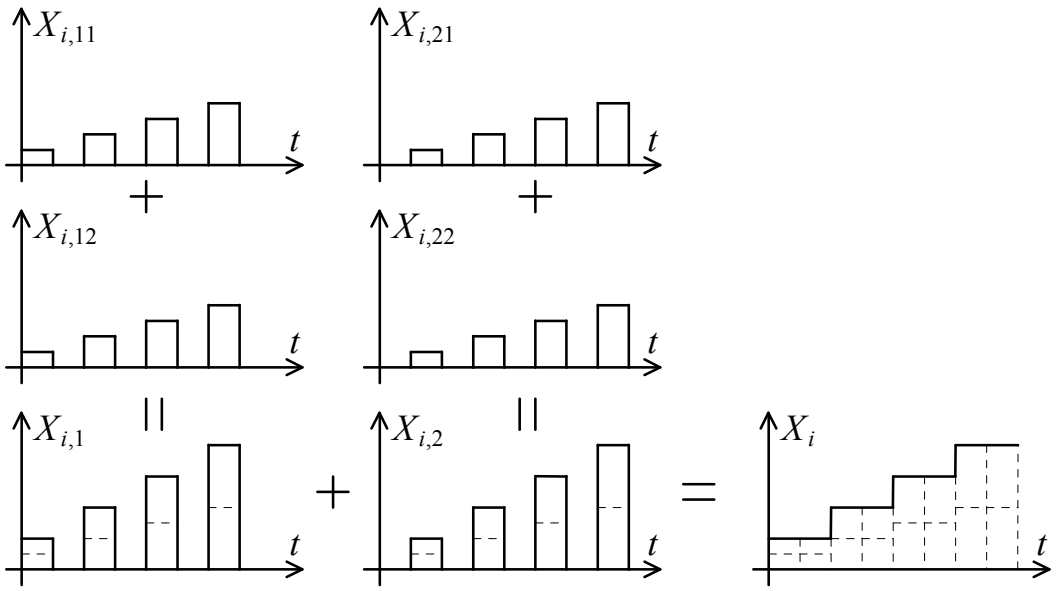
Current memory and current mirror.

Operation of SI Circuits

- Switched-current filters operate as periodically switched linear networks, where ideally the circuit reaches a static steady state between the switching instants.
- This mode of operation is essentially the same of the switched-capacitor filters.
- In switched-capacitor filters, the signal is represented by capacitor voltages, and the computations are done by charge balancing at the switching instants.
- In switched-current filters, the signal is represented by currents, and the computations are done by current balancing between the switching instants.
- For large signals, SI circuits exhibit a true current mode operation, with only currents being linear functions of the input signal. Voltages are related to the input by compressing nonlinear functions.
- Due to the simpler structures, SI circuits can operate using less energy, less area, and faster than equivalent SC circuits, although with possibly less precision, because good transistor matching is more difficult to achieve than good capacitance matching.

Signals in SI Circuits

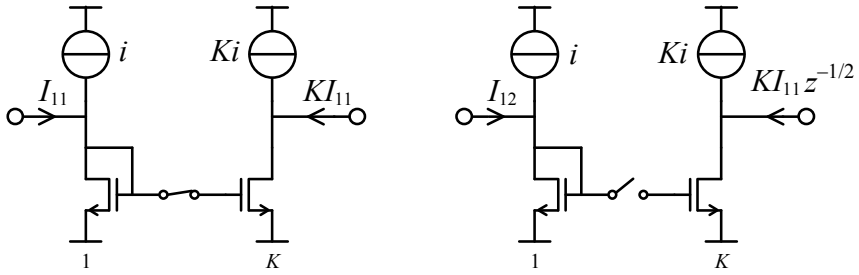
- A switching period is divided in a number f of phases.
- Each signal X_i in the filter is composed by f components $X_{i,m}$, each one for the m=1,...,f phases.
- Each $X_{i,m}$ is composed by another f components
- $X_{i,mk}$, each for one of the k=1,...,f phases of the input signal.
- These $f \times f$ components add together to form the signal X_i.
- In the example, a signal in a circuit with two phases.



Signal composition in a 2-phases system.

First-Generation Current Sample and Hold Cell

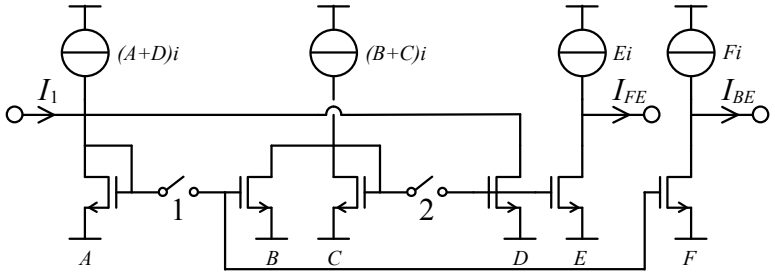
- In phase 1, a diode-connected transistor is used to generate the gate voltage of the output transistor, forming a current mirror.
- In phase 2, the output transistor retains the current of phase 1. The input current continues to flow through the input transistor, but is not sampled, and the output current is not affected by it.
- Note the notation in z-transform, meaning that the output current in phase 2 is a delayed copy (one phase) of the phase 1 output.



Phase 1: sample; Phase 2_ hold.

First-Generation SI Integrator

- Two sample-and-hold delay cells in a loop form an integrator, with two possible outputs, obtained by current mirrors:
- A backward Euler integrator at I_{FE} if $(BD)/(AC)=1$.
- A forward Euler integrator at I_{BE} if $(BD)/(AC)=1$.
- Advantage: Simple clocking system, with two nonoverlapping clock signals.
- Problem: Requires precise matching of two transistor pairs.

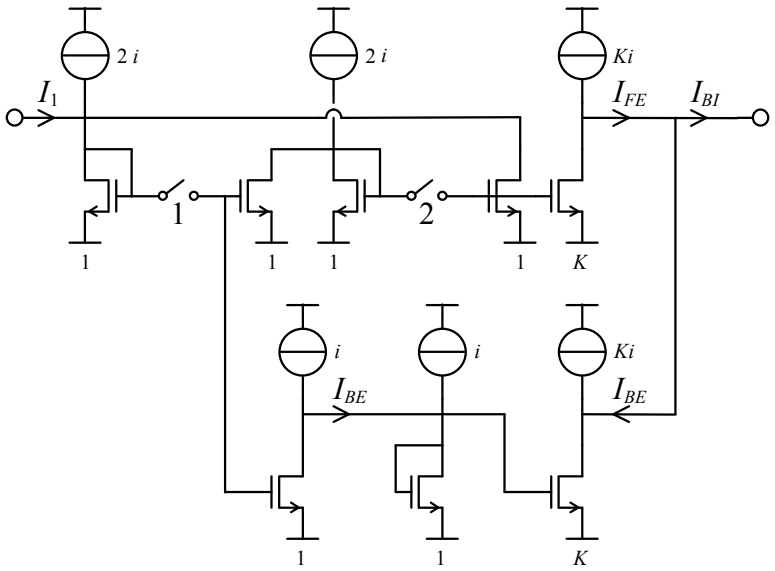


$$\frac{I_{FE,1}}{I_{1,1}} = \frac{\frac{B}{A}\frac{E}{C}z^{-1}}{1-\frac{B}{A}\frac{D}{C}z^{-1}}$$

$$\frac{I_{BE,1}}{I_{1,1}} = \frac{-\frac{F}{A}}{1-\frac{B}{A}\frac{D}{C}z^{-1}}$$

First-Generation Bilinear SI Integrator

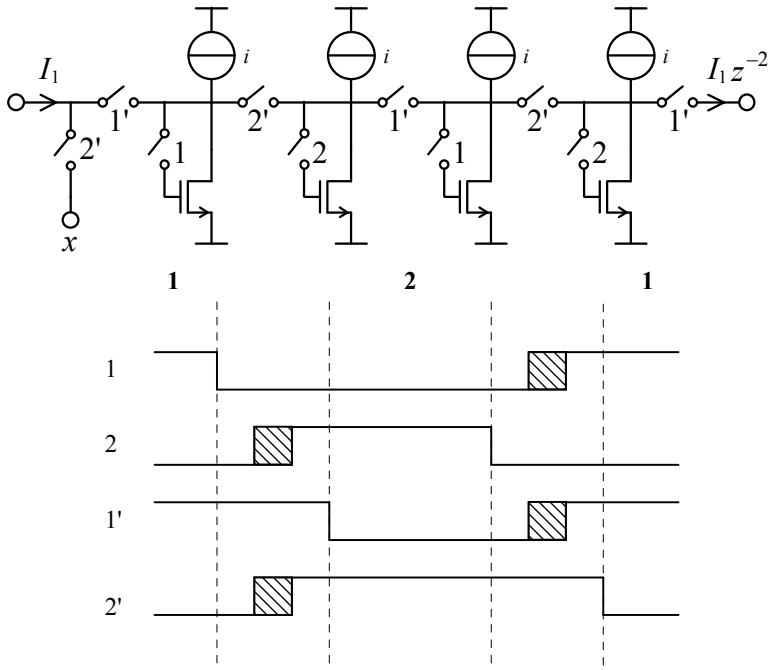
- A bilinear integrator can be built by the subtraction of an inverting BE output from a noninverting FE integrator.
- An inverting version is obtained by placing the current inverter at the FE output.
- Bilinear integrators allow precise filter realizations by transformation of passive prototypes.
- Many precise transistor matchings are required for a precise integrator.



$$\frac{I_{BI,1}}{I_{i,1}} = K\frac{1+z^{-1}}{1-z^{-1}}$$

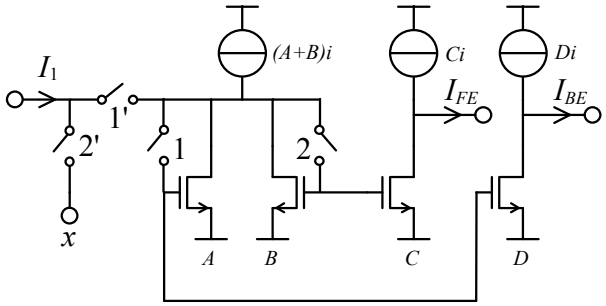
Second-Generation Current Sample and Hold Cell

- The same transistor is used as memory element and as output driver.
- There is no need of transistor matching to realize a unity-gain delay.
- A four-phases switching system is required for correct operation. (The same required by the integrators. Details ahead.)
- The figure shows a four-cell delay, realizing a delay of two switching periods.



Second-Generation SI Integrators

- Two delays in a loop form an integrator, with a pair of switches simplifying to a direct connection.
- Backward and forward Euler integrations are available, as in the first-generation circuit.
- The lossless integration do not depend on transistor matching.
- A four-phases clocking system is also required.
- Cascading of integrators requires the switch 2', to provide a path for the input current in phase 2.

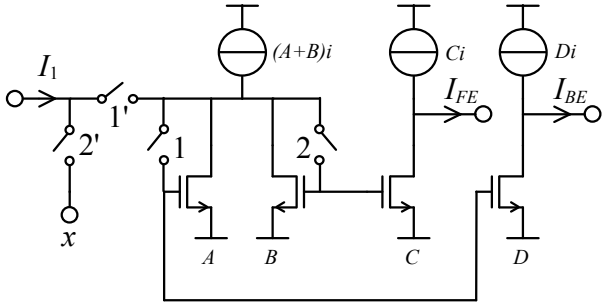


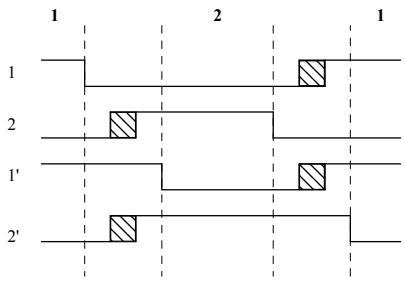
$$\frac{I_{FE,1}}{I_{1,1}} = \frac{\frac{C}{B} z^{-1}}{1 - z^{-1}}$$

$$\frac{I_{BE,1}}{I_{1,1}} = \frac{-\frac{D}{A}}{1 - z^{-1}}$$

Switching Sequence for Second-Generation SI Circuits

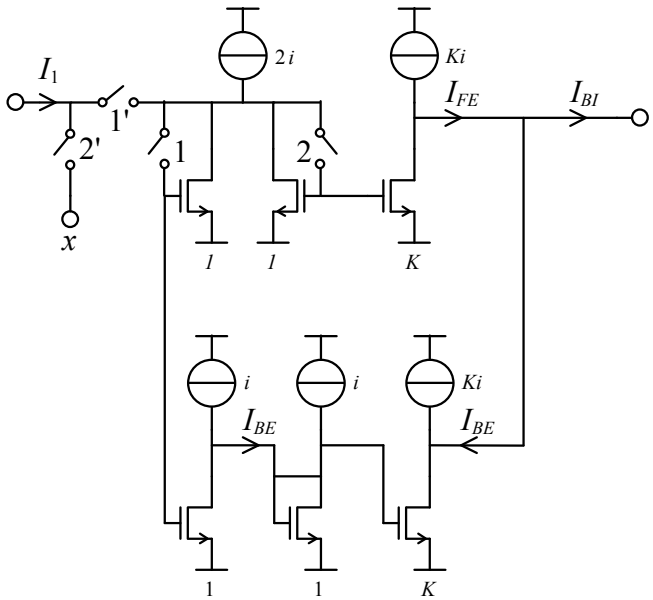
- Memory switches 1 and 2 must be opened at the start of the phase transitions, or the memorized currents are lost.
- Switches 1' and 2' open at the end of the transitions, because currents must always have a place to go, or large voltage spikes occur.
- Transistors must never leave the saturation region, or the input capacitance changes, invalidating current copies through current mirrors (hence the need of 2').
- Point *x* is a low-impedance point at the middle of the power supply voltage.





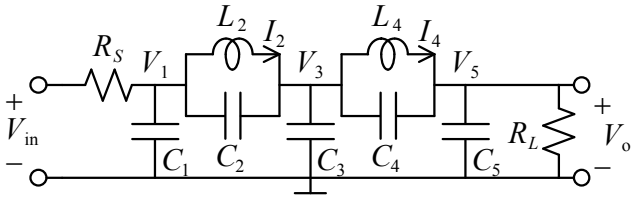
Second-Generation SI Bilinear Integrator

- A bilinear integrator can be built by the subtraction of an inverting BE output from a noninverting FE integrator, exactly as done with the first-generation circuit..
- An inverting version is obtained by placing the current inverter at the FE output.
- Precise matching is required for the correct realization of the numerator (not critical). The denominator is exact.



$$\frac{I_{BI,1}}{I_{i,1}} = K\frac{1+z^{-1}}{1-z^{-1}}$$

Filter Synthesis by the Simulation of Passive Prototypes



- The best prototypes are LC doubly-terminated ladder structures designed for maximum power transfer. A low-pass filter is used as example.
- This results in very low passband sensitivities, because errors in the reactive elements can only decrease the gain at the maximum power transfer frequencies, causing zero gain sensitivities for all Ls and Cs at these frequencies.
- The first step in the "leapfrog" technique is to obtain a system of (modified) state equations.

$$V_1 = \frac{\left(\frac{V_{in}}{R_S} - I_2 - \frac{V_1}{R_S}\right)}{s(C_1 + C_2)} + \frac{C_2 V_3}{C_1 + C_2}$$

$$I_2 = \frac{1}{sL_2}(V_1 - V_3)$$

$$V_3 = \frac{(I_2 - I_4)}{s(C_2 + C_3 + C_4)} + \frac{C_2 V_1 + C_4 V_5}{C_2 + C_3 + C_4}$$

$$I_4 = \frac{1}{sL_4}(V_3 - V_5)$$

$$V_5 = \frac{\left(I_4 - \frac{V_5}{R_L}\right)}{s(C_4 + C_5)} + \frac{C_4 V_3}{C_4 + C_5}$$

Generation of SI True Bilinear Filters

- The application of the bilinear transformation to the continuous-time equations results in the equations shown.
- From the equations, the transistor ratios for a unscaled SI filter are easily obtained.
- The “state variables” are represented by the difference between the transistor currents and their bias currents.

$$V_1 = \frac{\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(\frac{V_{in}}{R_S} - I_2 - \frac{V_1}{R_S}\right)}{C_1 + C_2} + \frac{C_2 V_3}{C_1 + C_2}$$

$$I_2 = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\frac{1}{L_2}\left(V_1 - V_3\right)$$

$$V_3 = \frac{\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(I_2 - I_4\right)}{C_2 + C_3 + C_4} + \frac{C_2 V_1 + C_4 V_5}{C_2 + C_3 + C_4}$$

$$I_4 = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\frac{1}{L_4}\left(V_3 - V_5\right)$$

$$V_5 = \frac{\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(I_4 - \frac{V_5}{R_L}\right)}{C_4 + C_5} + \frac{C_4 V_3}{C_4 + C_5}$$

$$I_1 = (T / R_S / (C_1 + C_2) / 2) V_{in}$$

$$A = C_4 / (C_2 + C_3 + C_4)$$

$$B = T / R_L / (C_4 + C_5) / 2$$

$$C = T / L_4 / 2$$

$$D = T / (C_4 + C_5) / 2$$

$$E = T / (C_2 + C_3 + C_4) / 2$$

$$F = C_2 / (C_1 + C_2)$$

$$G = C_4 / (C_4 + C_5)$$

$$H = T / L_4 / 2$$

$$I = T / L_2 / 2$$

$$J = T / (C_2 + C_3 + C_4) / 2$$

$$K = T / (C_1 + C_2) / 2$$

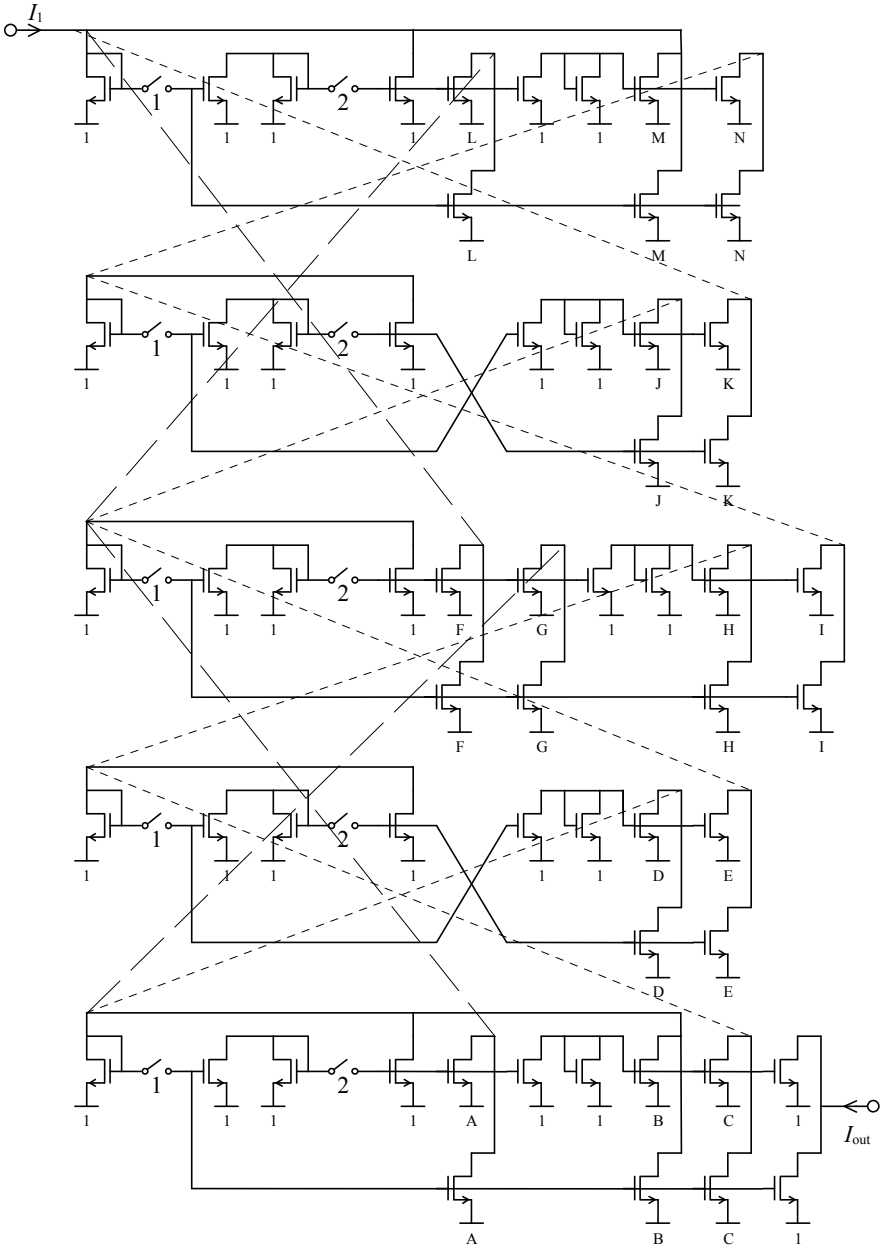
$$L = C_2 / (C_2 + C_3 + C_4)$$

$$M = T / R_G / (C_1 + C_2) / 2$$

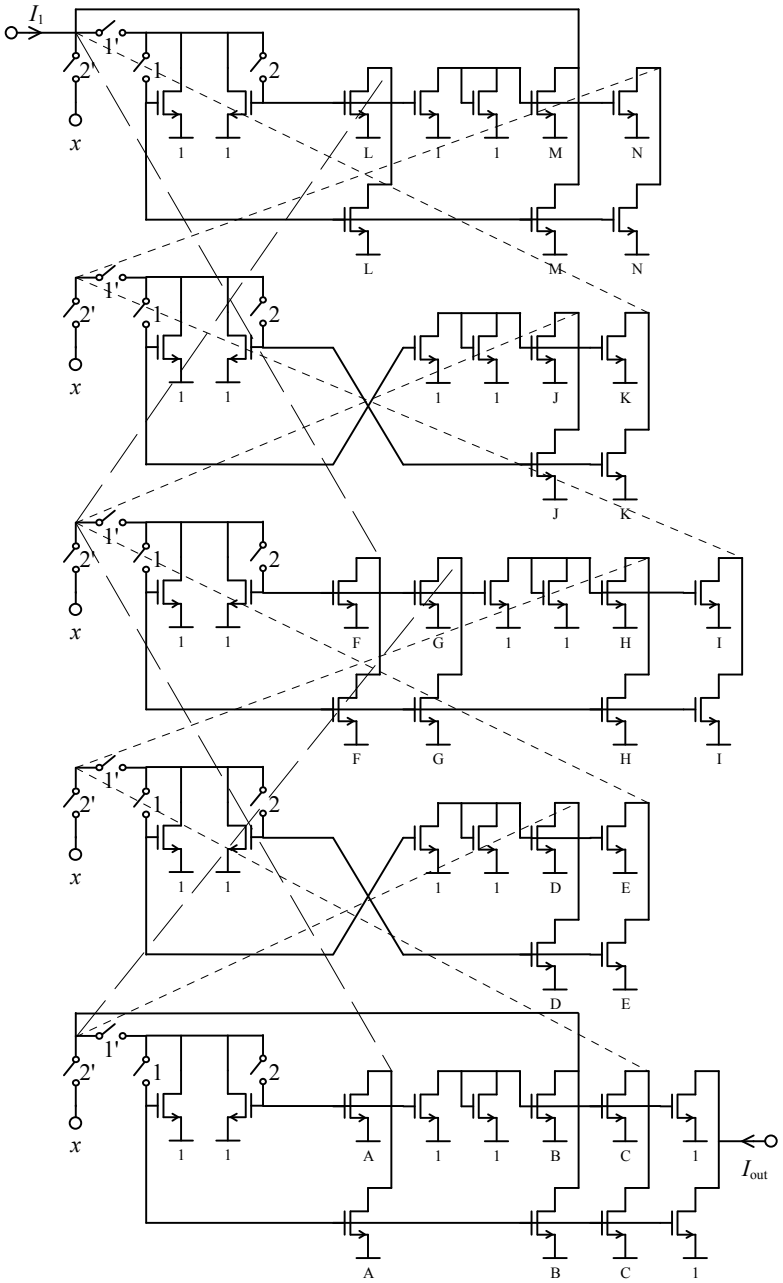
$$N = T / L_2 / 2$$

First-Generation Low-Pass True Bilinear Filter

(Bias sources omitted)

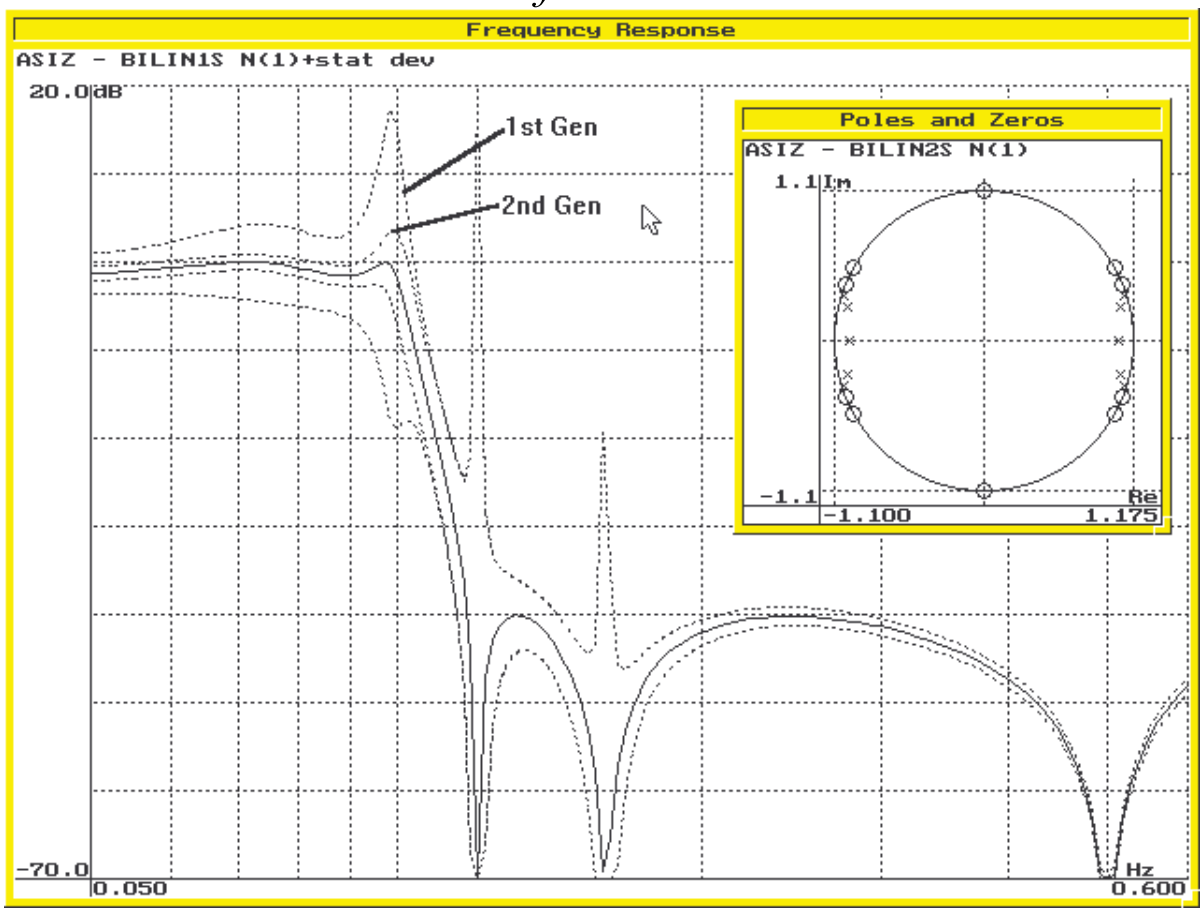


Second-Generation Low-Pass True Bilinear Filter



Sensitivity Comparison:

First-Generation × second-Generation true bilinear filters

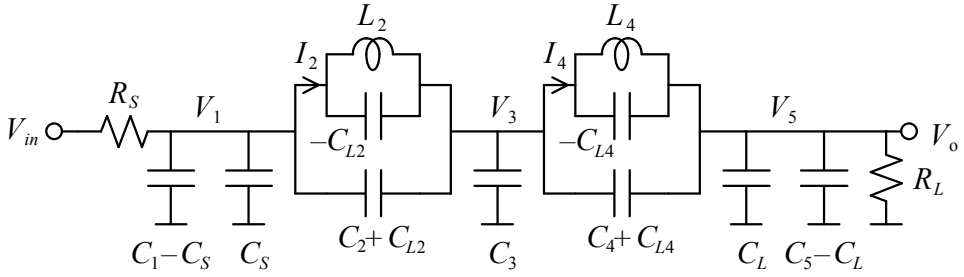


Gain statistical deviation for 5% mismatches in the mirrors (ASIZ program).

- The passband errors for the 1st-generation filter are significantly higher. The structures are identical except for the integrators.
- The valid output (curves above) is at phase 1. The complete output does not result in a bilinear filter (the zeros are at $z^{1/2} = -1$), but is a good approximation.

Bilinear SI filters built with Euler integrators

- Special circuit transformations in the prototype transform the bilinear integrations in the modified state equations into Euler integrations.



$$V_1 = \frac{\frac{V_{in}}{R_S} - \frac{V_1}{R_S} - sC_S V_1 - I_2 + s\left(C_2 + C_{L2}\right)V_3}{s\left(C_1 + C_2 + C_{L2} - C_S\right)}$$

$$I_2 = \left(\frac{1}{sL_2} - sC_{L2}\right)\left(V_1 - V_3\right)$$

$$V_3 = \frac{I_2 - I_4 + s\left(C_2 + C_{L2}\right)V_1 + s\left(C_4 + C_{L4}\right)V_5}{s\left(C_2 + C_3 + C_4 + C_{L2} + C_{L4}\right)}$$

$$I_4 = \left(\frac{1}{sL_4} - sC_{L4}\right)\left(V_3 - V_5\right)$$

$$V_5 = \frac{I_4 - \frac{V_5}{R_L} - sC_L V_5 + s\left(C_4 + C_{L4}\right)V_3}{s\left(C_4 + C_5 + C_{L4} - C_L\right)}$$

- The introduced elements are:

$$C_S = \frac{T}{2R_S}, \quad C_{L2} = \frac{T^2}{4L_2}, \quad C_{L4} = \frac{T^2}{4L_4}, \quad C_L = \frac{T}{2R_L}$$

- Applying the bilinear transformation to the continuous-time equations, a set of equations with Euler integrations results. Only one bilinear integration remains (the one of the input, that can be moved to the output).

$$V_1 = \frac{\frac{T}{1-z^{-1}}\left(\frac{V_{in}}{R_S}\frac{1+z^{-1}}{2} - I_2' - \frac{V_1}{R_S}\right)}{C_1 + C_2 + C_{L2} - C_S} + \frac{(C_2 + C_{L2})V_3}{C_1 + C_2 + C_{L2} - C_S}$$

$$I_2' = I_2\frac{1+z^{-1}}{2} = \frac{Tz^{-1}}{1-z^{-1}}\frac{1}{L_2}(V_1 - V_3)$$

$$V_3 = \frac{\frac{T}{1-z^{-1}}(I_2' - I_4')}{C_2 + C_3 + C_4 + C_{L2} + C_{L4}} + \frac{(C_2 + C_{L2})V_1 + (C_4 + C_{L4})V_5}{C_2 + C_3 + C_4 + C_{L2} + C_{L4}}$$

$$I_4' = I_4\frac{1+z^{-1}}{2} = \frac{Tz^{-1}}{1-z^{-1}}\frac{1}{L_4}(V_3 - V_5)$$

$$V_5 = \frac{\frac{T}{1-z^{-1}}\left(I_4' - \frac{V_5}{R_L}\right)}{C_4 + C_5 + C_{L4} - C_L} + \frac{(C_4 + C_{L4})V_3}{C_4 + C_5 + C_{L4} - C_L}$$

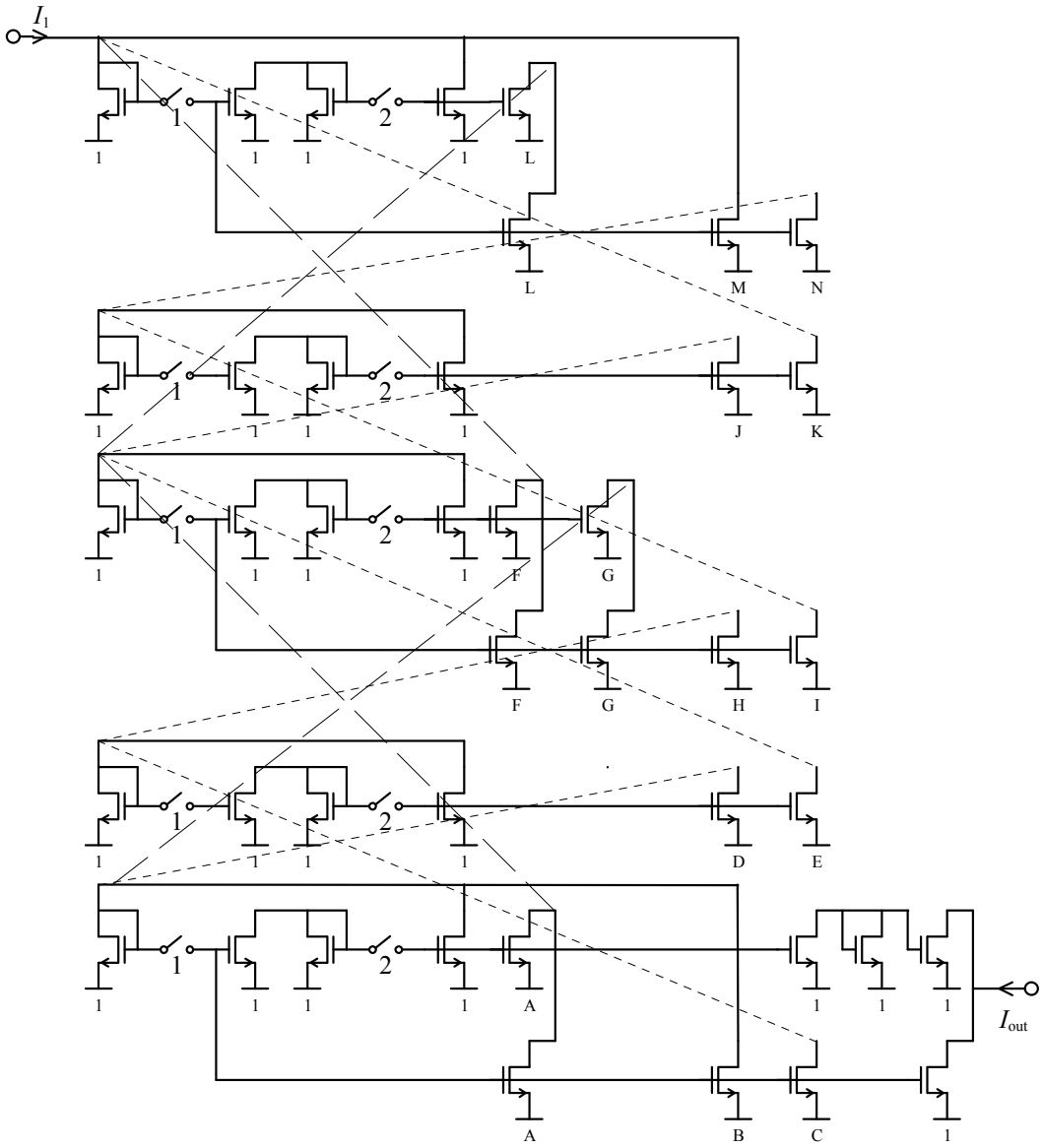
The circuit transformations cause:

- The equations corresponding to the capacitor voltages are transformed into backward Euler integrations.
- The equations corresponding to the inductor currents (LC tanks) are transformed into forward Euler integrations.

Transistor ratios:

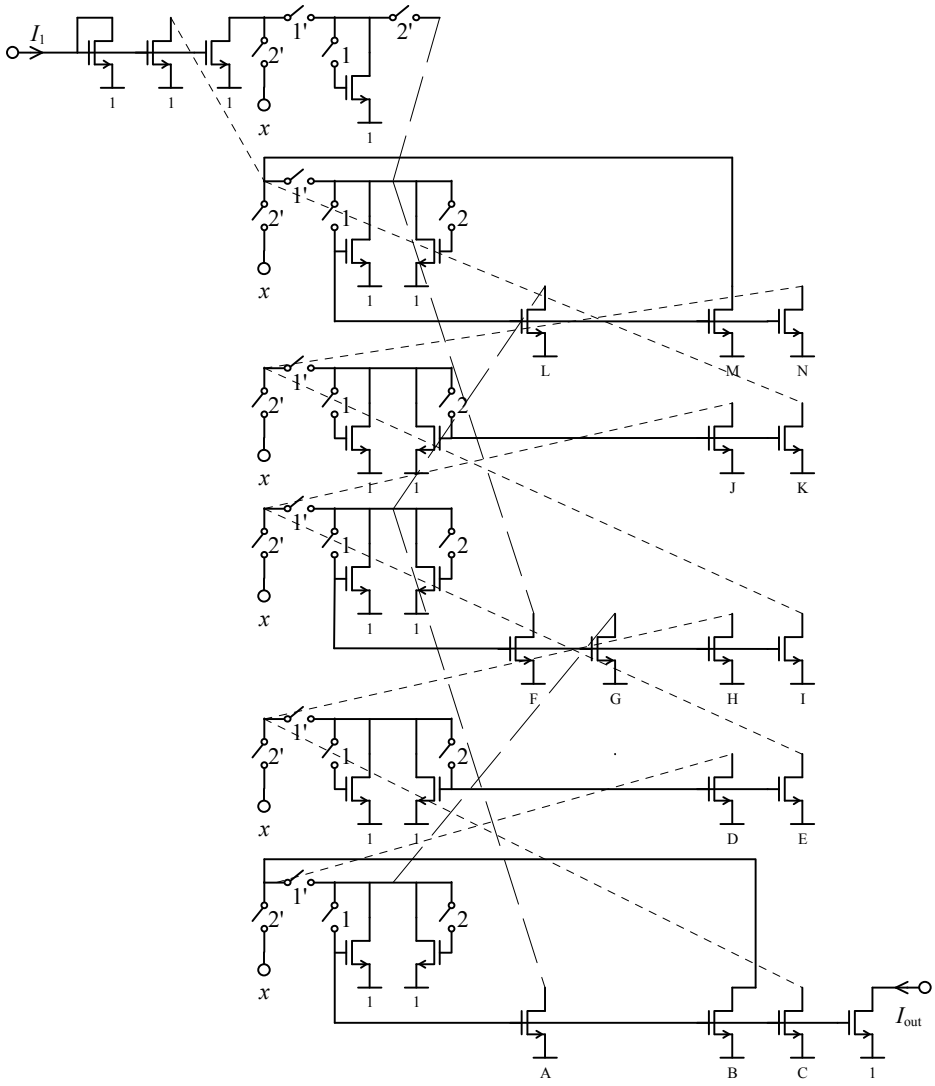
$$I_{in} = T / R_G / (C_1 + C_2 + C_{L2} - C_S) V_{in}$$
$$A = (C_4 + C_{L4}) / (C_2 + C_3 + C_4 + C_{L2} + C_{L4})$$
$$B = T / R_L / (C_4 + C_5 + C_{L4} - C_L)$$
$$C = T / L_4$$
$$D = T / (C_4 + C_5 + C_{L4} - C_L)$$
$$E = T / (C_2 + C_3 + C_4 + C_{L2} + C_{L4})$$
$$F = (C_2 + C_{L2}) / (C_1 + C_2 + C_{L2} - C_S)$$
$$G = (C_4 + C_{L4}) / (C_4 + C_5 + C_{L4} - C_L)$$
$$H = T / L_4$$
$$I = T / L_2$$
$$J = T / (C_2 + C_3 + C_4 + C_{L2} + C_{L4})$$
$$K = T / (C_1 + C_2 + C_{L2} - C_S)$$
$$L = (C_2 + C_{L2}) / (C_2 + C_3 + C_4 + C_{L2} + C_{L4})$$
$$M = T / R_G / (C_1 + C_2 + C_{L2} - C_S)$$
$$N = T / L_2$$

First-Generation Bilinear Low-Pass Filter with Euler Integrators



Note the absence of inverters, except at the output circuit. The valid output is at phase 1 (as in the true bilinear circuit).

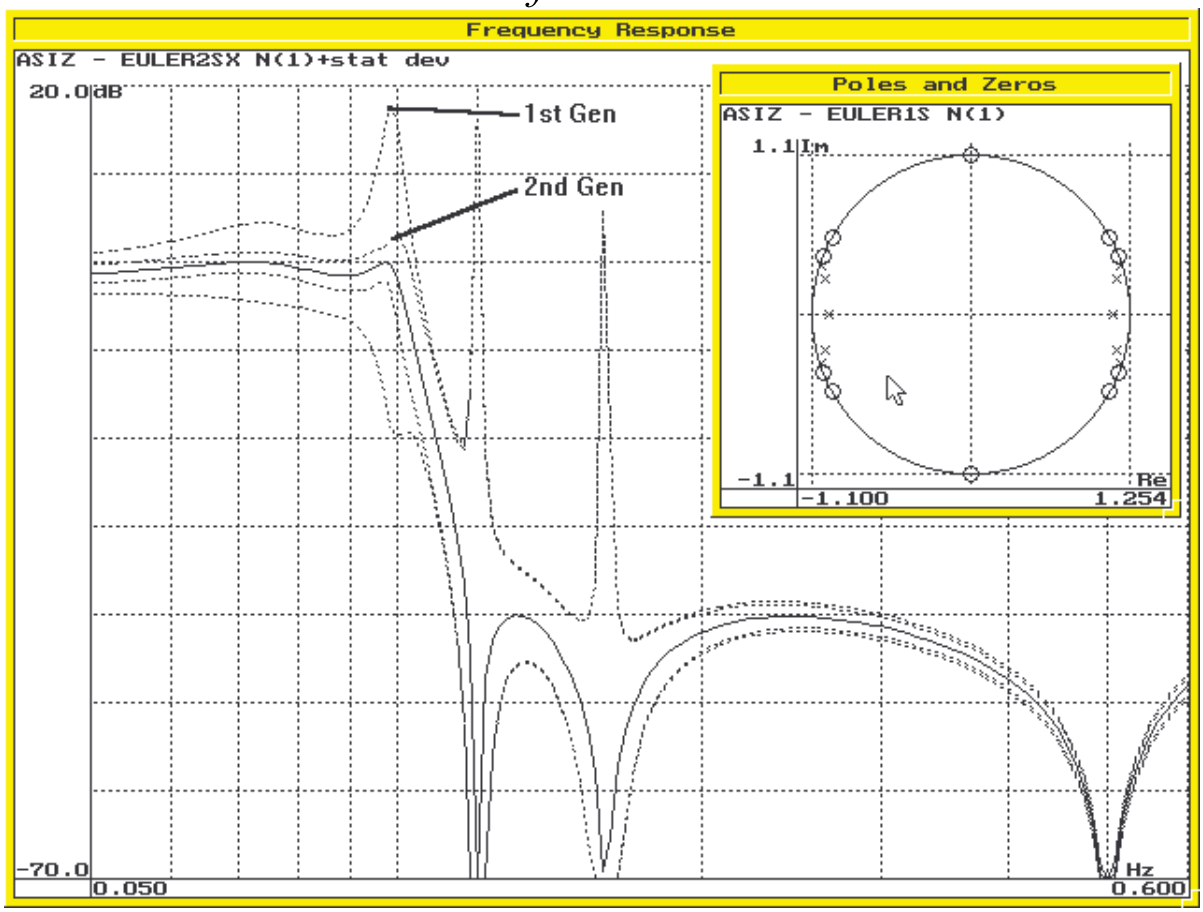
Second-Generation Bilinear Low-Pass Filter with Euler Integrators



Note the simplified direct coupling among the integrators and the bilinear integration of the input. The valid output is at phase 1. The output at phase 2 is a delayed copy. A solution similar to the 1st-generation structure is also possible, but requires more transistors.

Sensitivity Comparison:

First-generation × second generation bilinear/Euler filters.



Gain statistical deviation for 5% mismatches in the mirrors.

- The second-generation circuit also presents better sensitivity characteristics in this case.
- The realizations with Euler integrators are slightly more sensitive at the stopband than the equivalent true bilinear realizations. This is due to the introduced elements without correspondent in the passive prototype.

Component Simulation SI Technique

- A Gm-C circuit can be described by the nodal system (1), in Laplace transform.
- Applying the bilinear transformation (2) to (1), the system (3) results.
- The comparison between (1) and (3) gives the equivalencies (4), applicable to transcapacitances, transconductances, input currents, and voltages.
- The same can be done using Euler transformations. What change are the equivalencies for transconductances and inputs, that become (5) for the backward Euler and (6) for the forward Euler transformations.

(1) $s\mathbf{C}\mathbf{v}(s) + \mathbf{G}\mathbf{v}(s) + \mathbf{j} = \mathbf{0}$

(2) $s \to \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$

(3) $(1-z^{-1})\frac{\mathbf{C}}{T}\mathbf{v}(z) + (1+z^{-1})\frac{\mathbf{G}}{2}\mathbf{v}(z) + (1+z^{-1})\frac{1}{2}\mathbf{j}(z) = \mathbf{0}$

(4) $sC \to \left(1-z^{-1}\right)\frac{C}{T} \qquad G \to \left(1+z^{-1}\right)\frac{G}{2}$

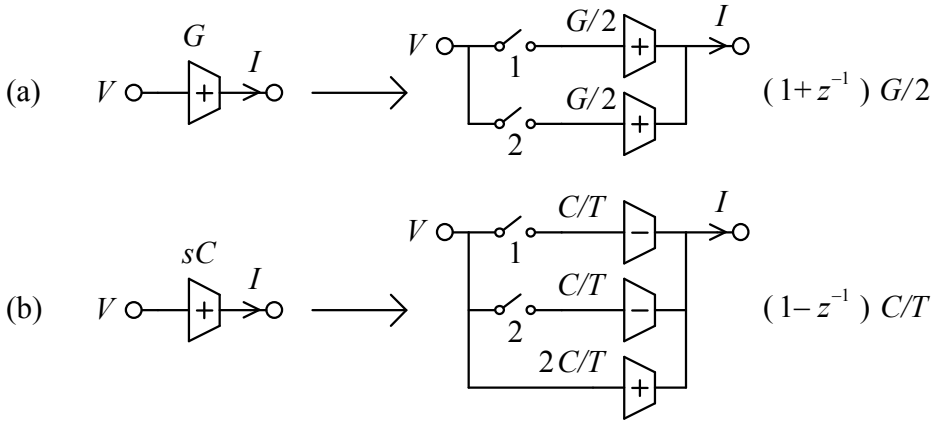
$j(s) \to \left(1+z^{-1}\right)\frac{1}{2}j(z) \quad v(s) \to v(z)$

(5) $G \to G \quad j(s) \to j(z)$

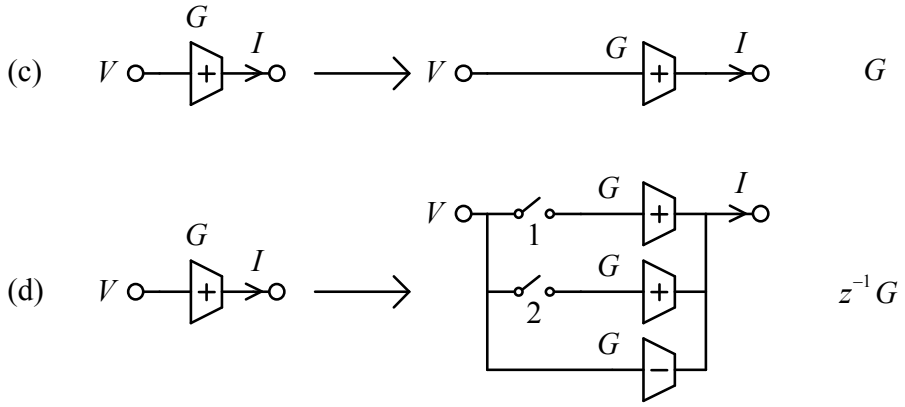
(6) $G \to \left(z^{-1}\right)G \quad j(s) \to \left(z^{-1}\right)j(z)$

Circuit Equivalents

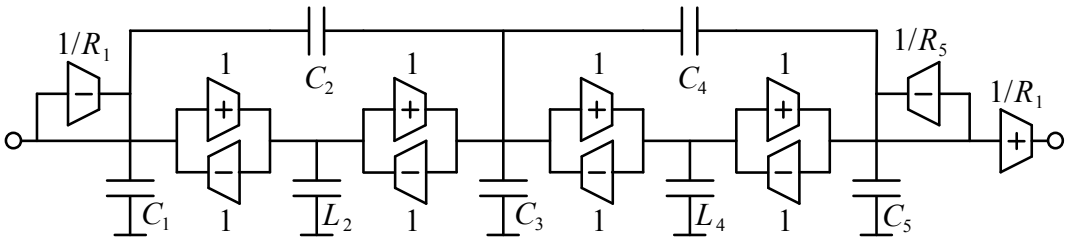
- Equivalent circuits to the bilinear transconductance (a) and transcapacitance (b) in (4) can be built using transconductors (with input capacitance) and switches.
- These circuits operate with doubled sampling rate and without current-conducting switches.
- A two-phases nonoverlapping clock system can be used.



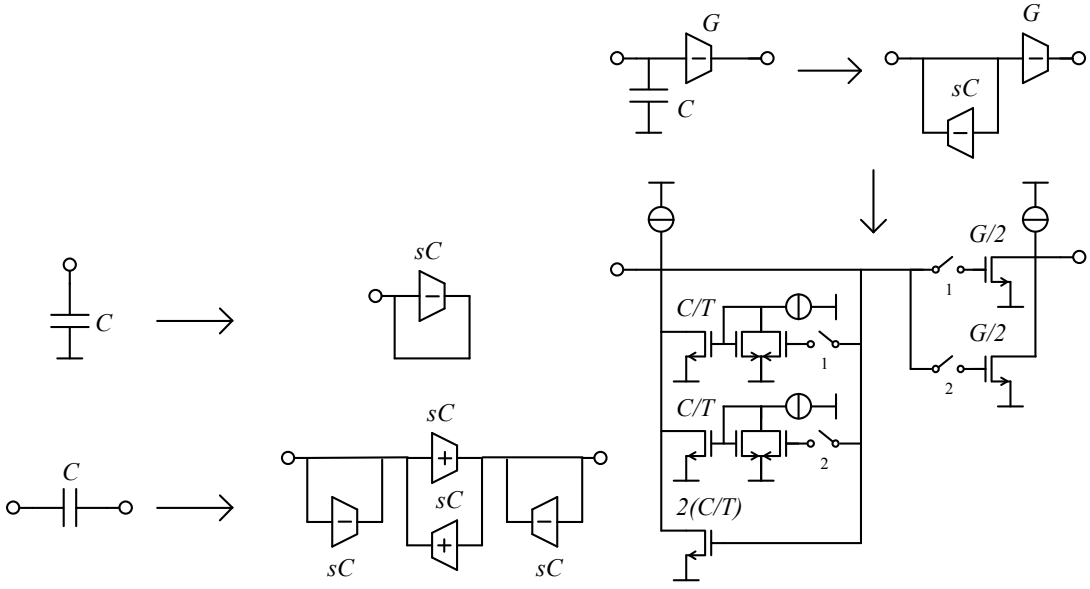
- The equivalencies for the backward Euler (c) and Forward Euler (d) transconductances are shown below.



Component Simulation of OTA-C Filters



Gm-C simulation of a 5th-order low-pass LC ladder filter, with current input and output.

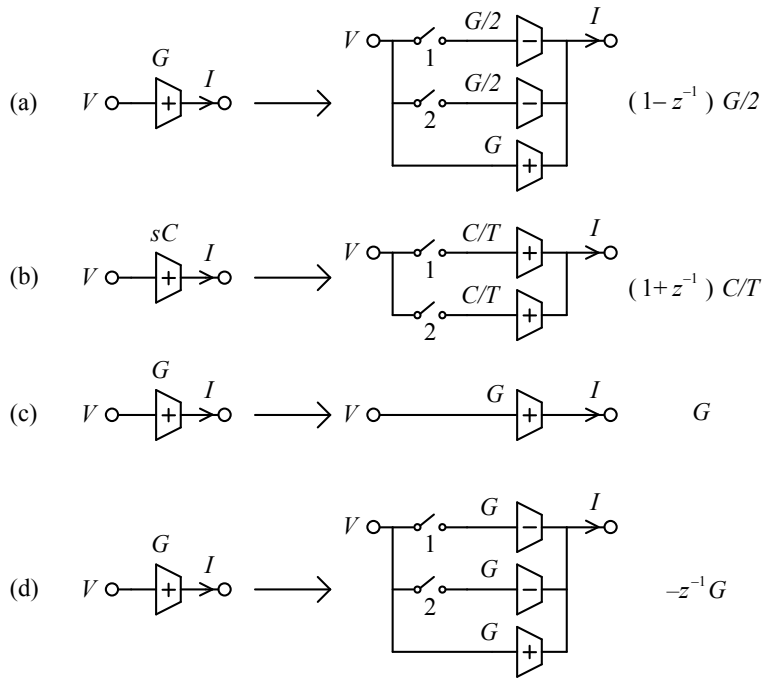


Simulations of grounded and floating capacitors using transcapacitances, and construction of a bilinear integrator (without simplifications).

- Any OTA-C structure can be simulated, what allows the reuse of all the structures developed for these filters.

CS Filters Using Modulated Signals

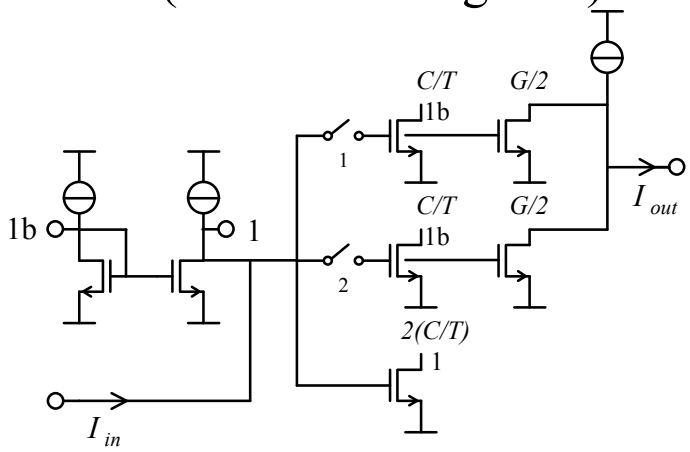
- The transcapacitance elements using three signal paths are very sensitive to component mismatches, with the generated error being proportional to T.
- If the filter is operated with modulated signals, that invert polarity at each phase, terms in z^{-1} must be realized with inverted polarity, what eliminates the continuous path in the transcapacitances.



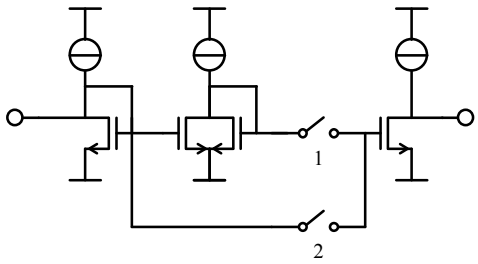
Transcapacitance (b) and transconductances for the bilinear (a), backward Euler (c) and forward Euler approximations, considering modulated signals.

General Implementation Scheme for Component-Simulation Structures

- It is possible to reduce the number of inverters and switches required by component-simulation structures to a minimum by implementing integrators as shown below (a bilinear integrator):

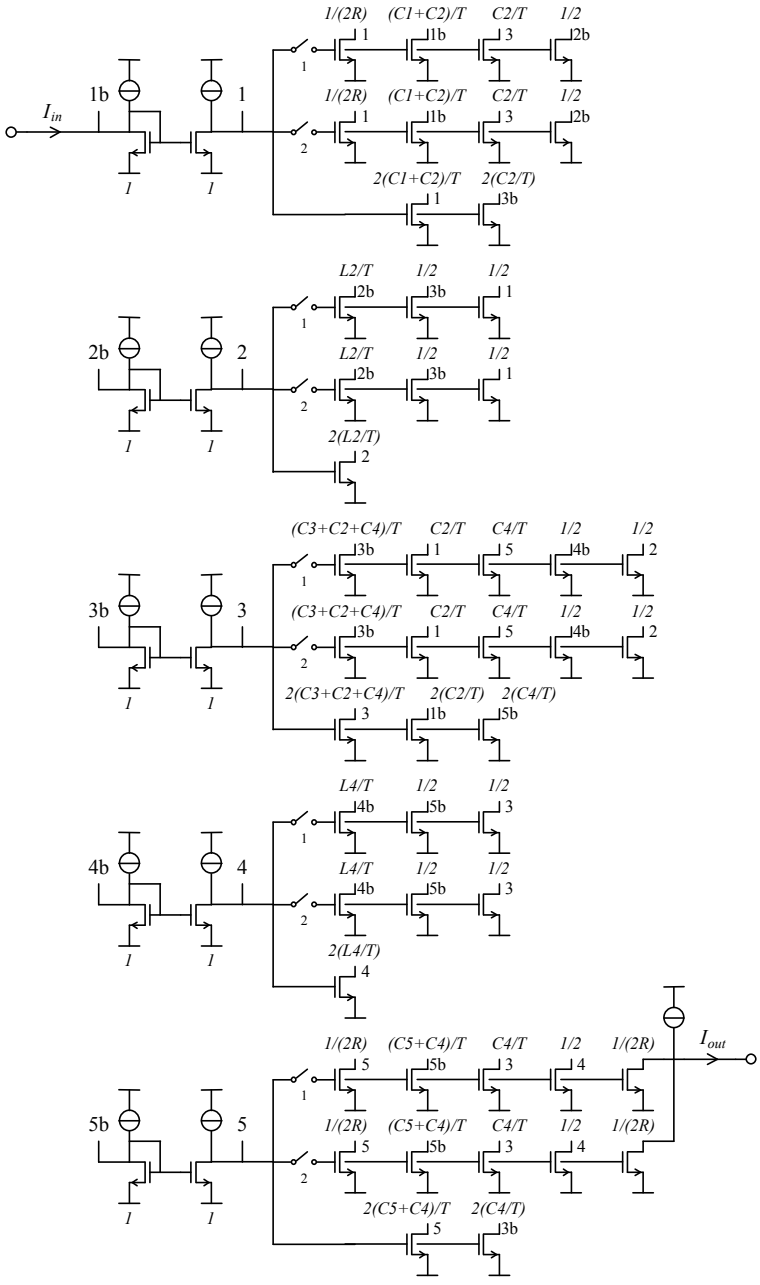


The inverters are moved to the input circuit, and all the connections are made to the inverting or to the noninverting inputs.

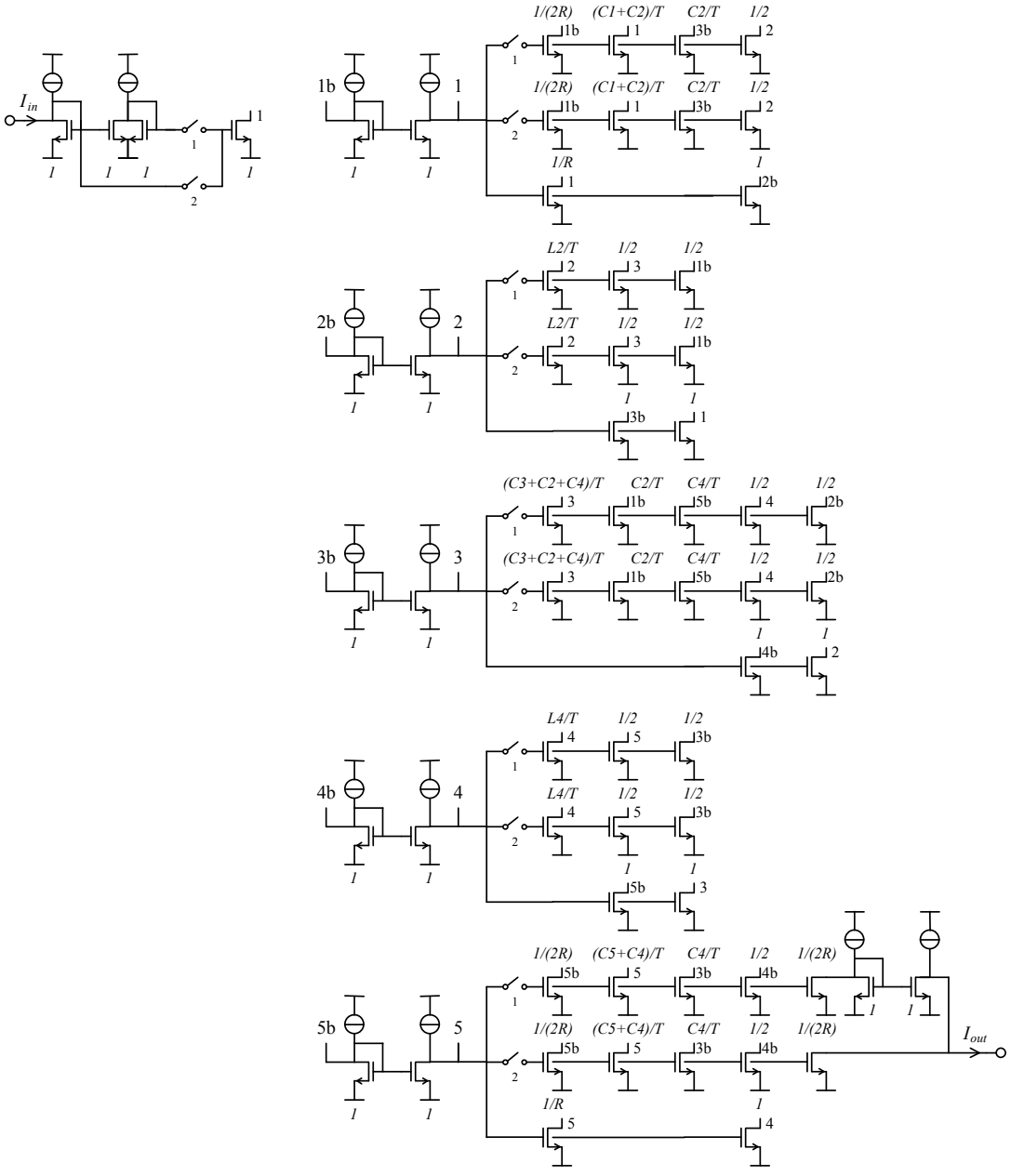


A current modulator, for use in modulated-signal filters. Simplifications are possible at the output circuit.

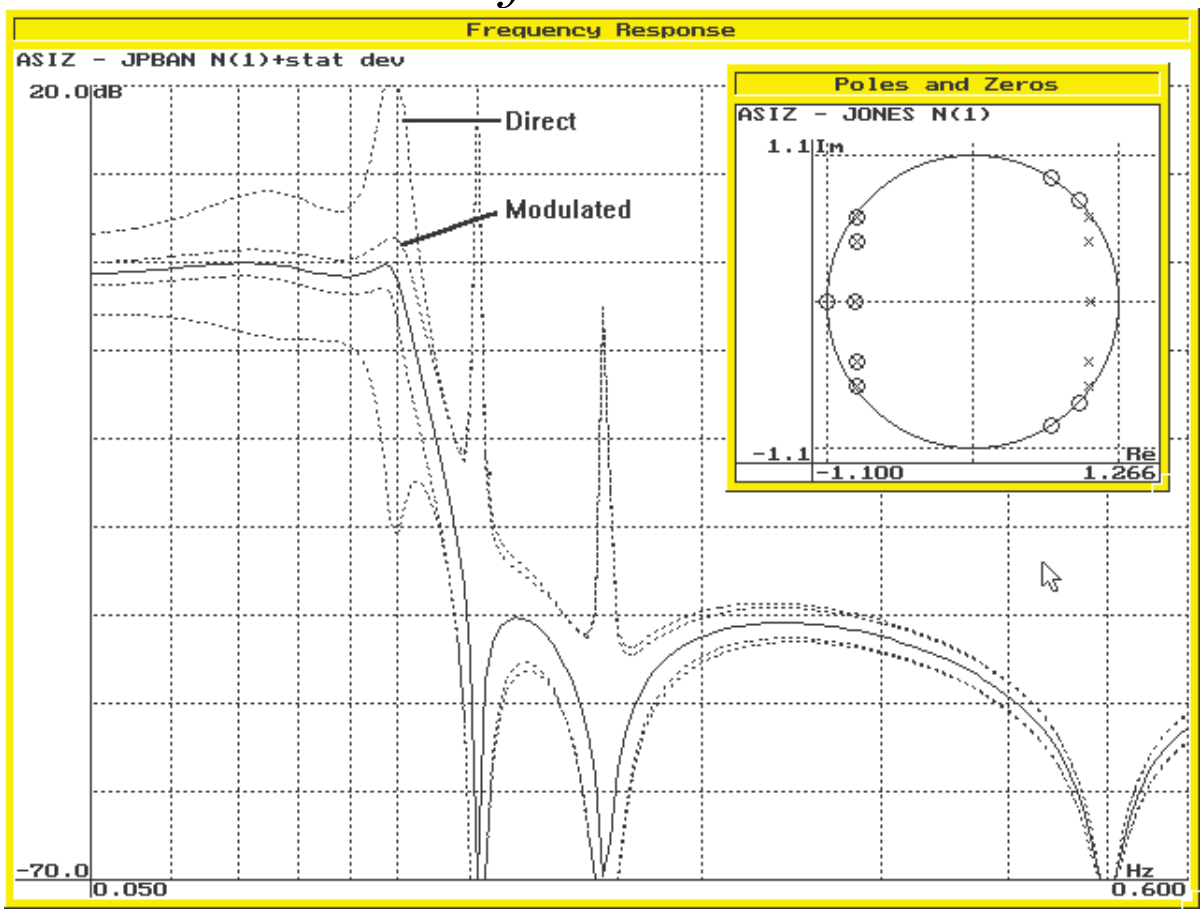
CS 5th-Order True Bilinear Low-Pass Filter - “Direct” Form



CS True Bilinear Low-Pass Filter - “Modulated” Form



Sensitivity Comparison: *"Direct" × "Modulated" CS SI filters*

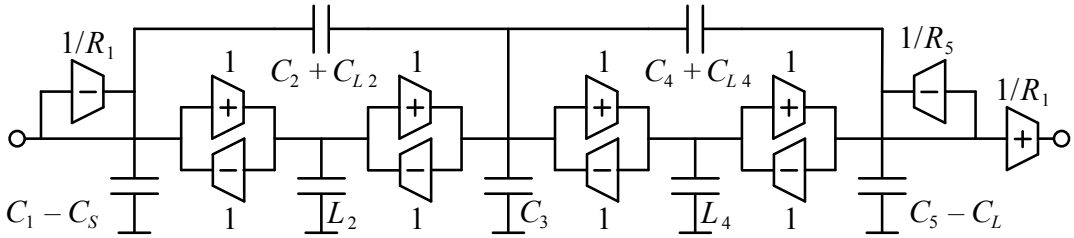


Gain deviations for 5% mismatch among the transistors.

- The direct version is very sensitive, but the modulated version is almost as insensitive as a second-generation filter. Both admit the simple clock system of a first-generation filter.
- The CS filters require only half of the sampling frequency of 1st and 2nd generation structures for identical responses.

CS Bilinear Filters Using Euler Integrators

- The same transformations derived for the 1st and 2nd-generation structures can be applied to CS structures. The OTA-C prototype becomes:

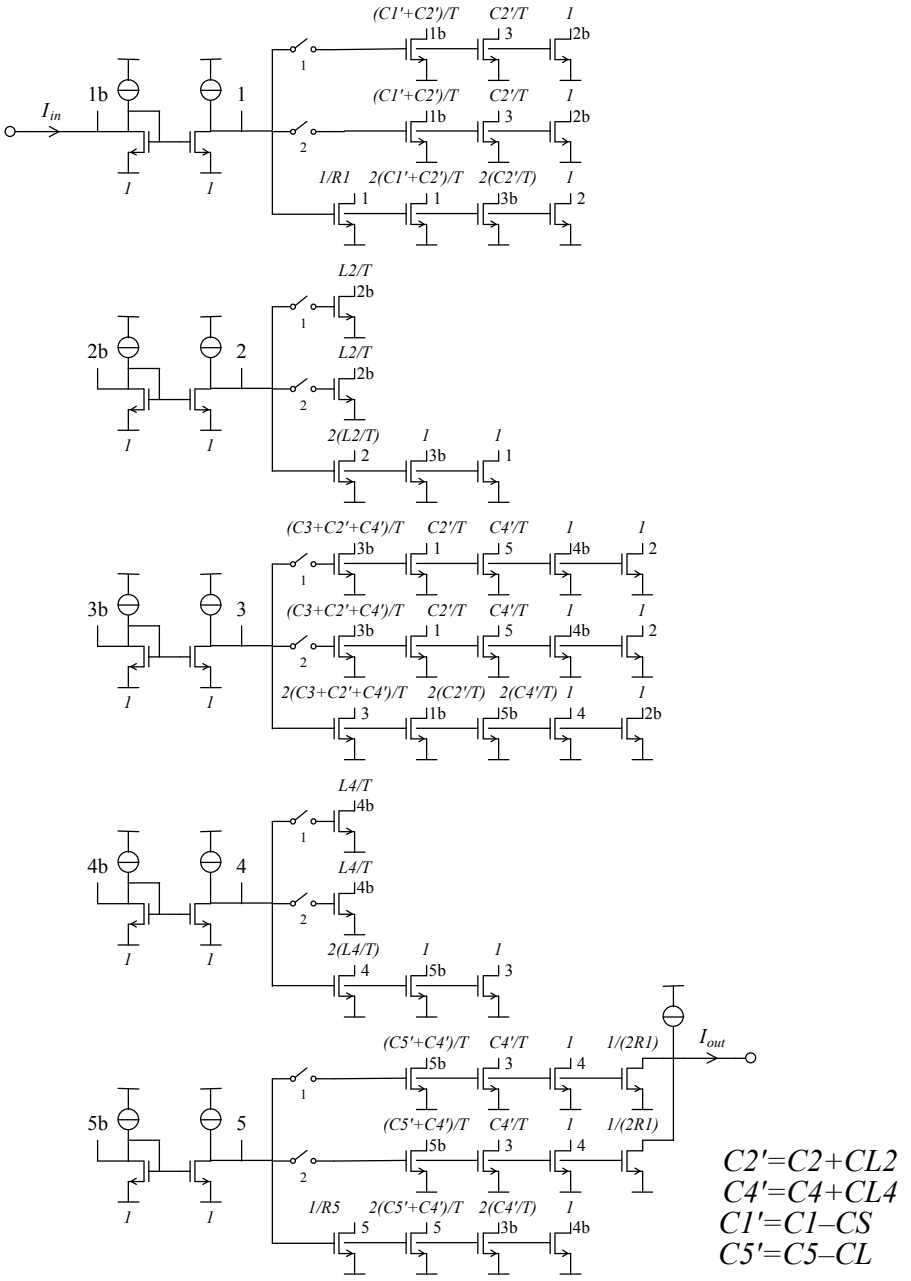


Where again:

$$C_S = \frac{T}{2R_1}, \quad C_{L2} = \frac{T^2}{4L_2}, \quad C_{L4} = \frac{T^2}{4L_4}, \quad C_L = \frac{T}{2R_5}$$

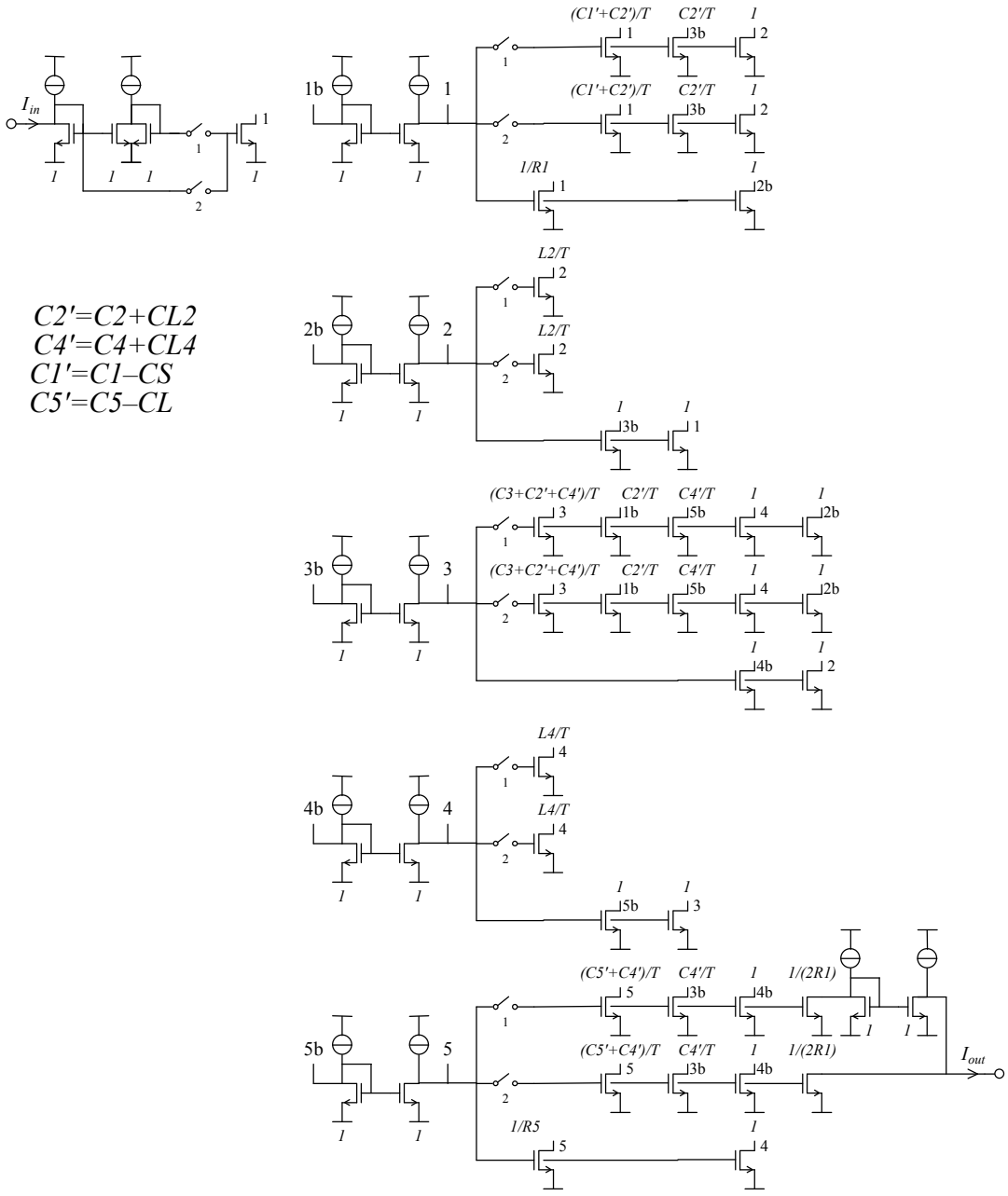
- All the integrators simulating capacitor voltages must be backward Euler integrators, and all the ones simulating inductor currents must be forward Euler integrators. The integrator type is defined by the type of the transconductor feeding the capacitor. One bilinear integration must exist at the input or output.
- Because the backward Euler integrators are very simple, some hardware simplification results, specially when the modulated version, the only practical, is used.

CS 5th-Order Bilinear Low-Pass Filter with Euler Integrators - “Direct” Form



$C2'=C2+CL2$
$C4'=C4+CL4$
$C1'=C1–CS$
$C5'=C5–CL$

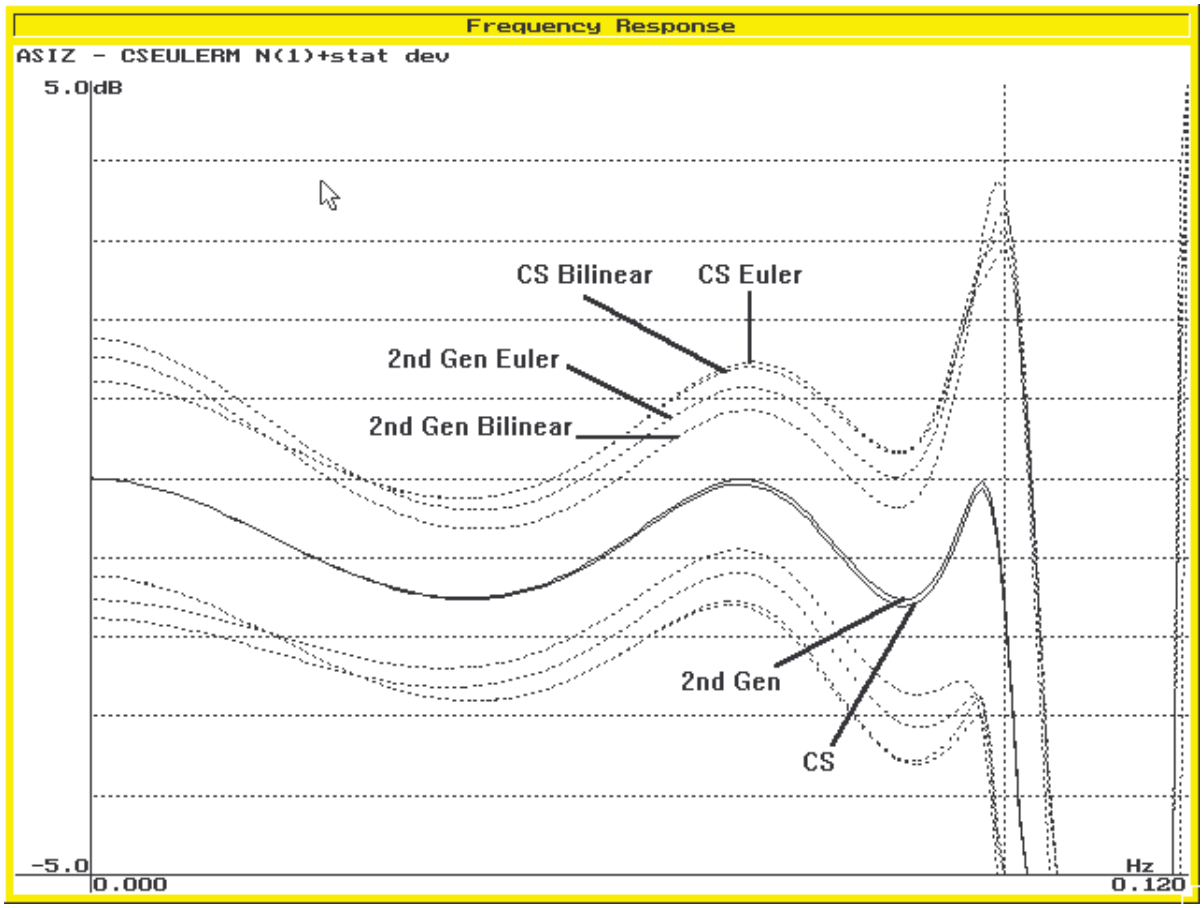
CS 5th-Order Bilinear Low-Pass Filter with Euler Integrators - “Modulated” Form



C2'=C2+CL2
C4'=C4+CL4
C1'=C1–CS
C5'=C5–CL

Sensitivity Comparison:

Second-Generation × Component-Simulation
Modulated Filters, True Bilinear and Euler/Bilinear.
Pass band.



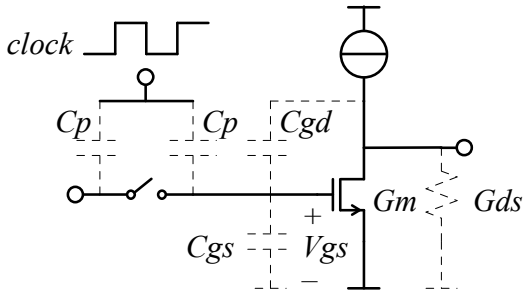
Pass-band error limits for 5% mismatches in a 5th-order elliptic filter.

- There is no significant difference between True Bilinear and Euler/Bilinear CS structures, but the later are simpler.
- Second-Generation True Bilinear structures are the best in terms of sensitivity.

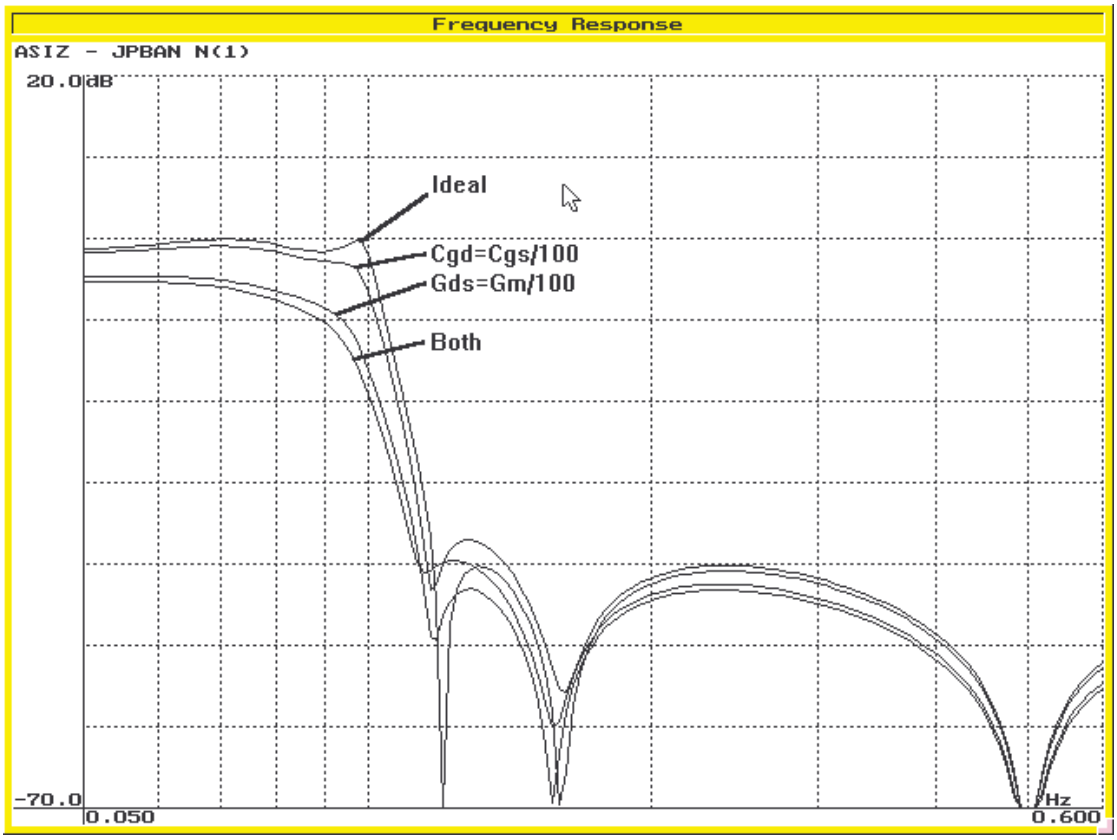
Imperfections and Compensation Techniques in SI Filters

The main sources of errors are:

- Insufficient *Gm*/*Gds* ratio of single MOS transistors: The current-transfer operations become inaccurate, and the general (linear) effect is a lowering of Q poles.
- Significant *Cgd* capacitances, or insufficient *Cgs*/*Cgd* ratio in single MOS transistors: Variations in *Vds* voltages introduce variations in *Vgs* voltages in transistors with open gate, what results in an effect similar to the effect of *Gds*.
- Clock feedthrough through the switch capacitances: The effect is particularly serious in SI circuits, because the clock signal affects (~linearly) the *Vgs* voltages, but the currents are nonlinear functions of these voltages, what causes nonlinear, signal-dependent effects.



Effect of Finite Gm/Gds and Cgs/Cgd Ratios

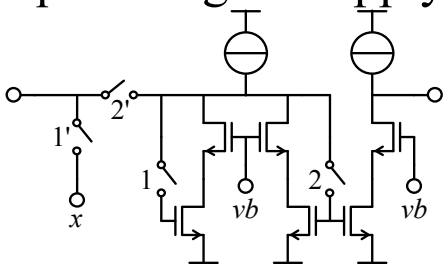


Loss effects in a CS modulated true bilinear filter.

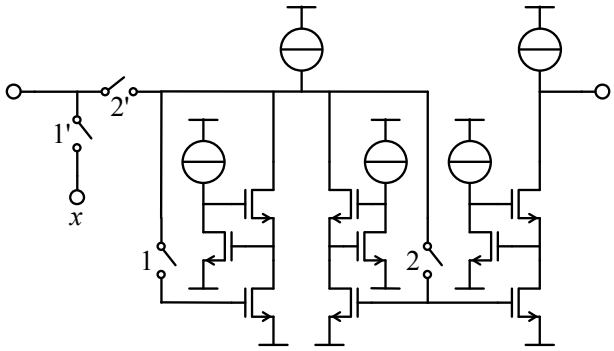
- Effects in other structures are similar. CS and 1st-generation structures are the least sensitive, but the difference to 2nd-generation structures is small.
- Note that the 1:100 ratios used in the simulation are about the maximum attainable with single transistors.

Compensations For Low Gm/Gds and Cgd/Cgs Ratios

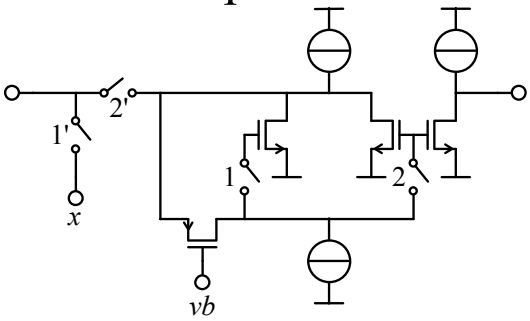
- Cascoded transistors: Decrease the effective *Gds* by ~(*Gm*/*Gds*)^2.Requires higher supply voltage.



- Regulated cascode structures: Decrease the effective *Gds* by ~(*Gm*/*Gds*)^3. Also requires higher supply voltage.

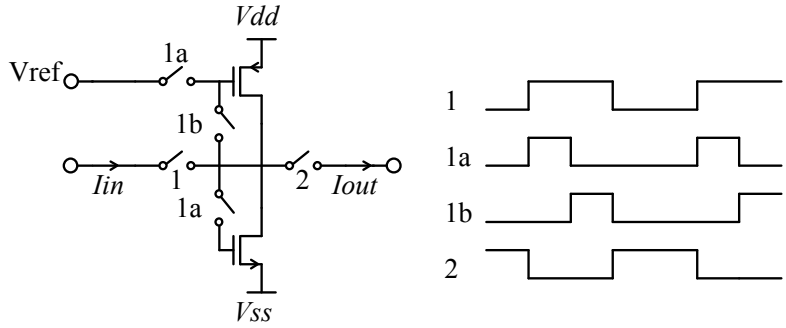


- Common-gate amplifier: Acts Increasing *Gm* instead of lowering *Gds*. Can operate with low voltage.



Compensations for Clock Feedthrough

- Dummy switches: Try to decrease the injected charge by extracting the same charge through other , dummy, switch, connected to the transistor gate and operated with an inverted clock signal.
- The "S^2I" technique: Reduces the problematic signal-dependent clock feedthrough using a double sampling technique. The upper transistor compensates the charge injected in the main transistor at the end of phase 1a, and the charge injected at the end of phase 1b in the upper transistor is almost signal-independent.



- Differential SI circuits: Try to reject the feedthrough signal with the use of the common-mode rejection of differential structures.
- Component-simulation structures using modulated signals eliminate a good part of the linear feedthrough signal by the inversion of the processed signal at each phase. What is injected in one phase is extracted in the next.

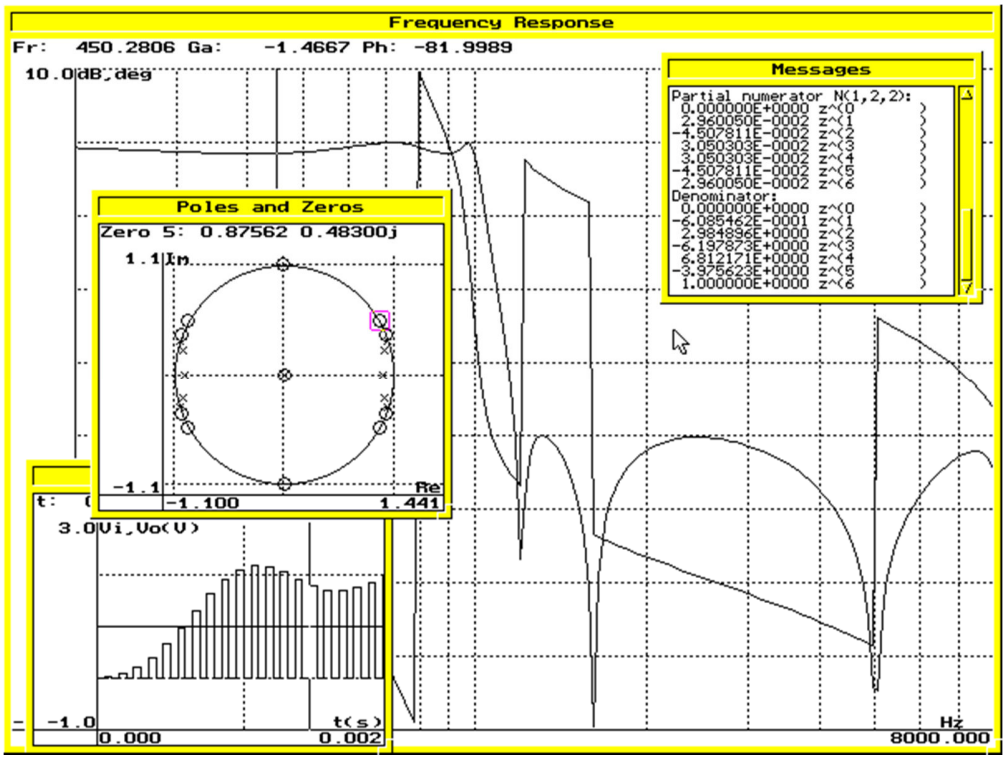
Simulation of SI Circuits

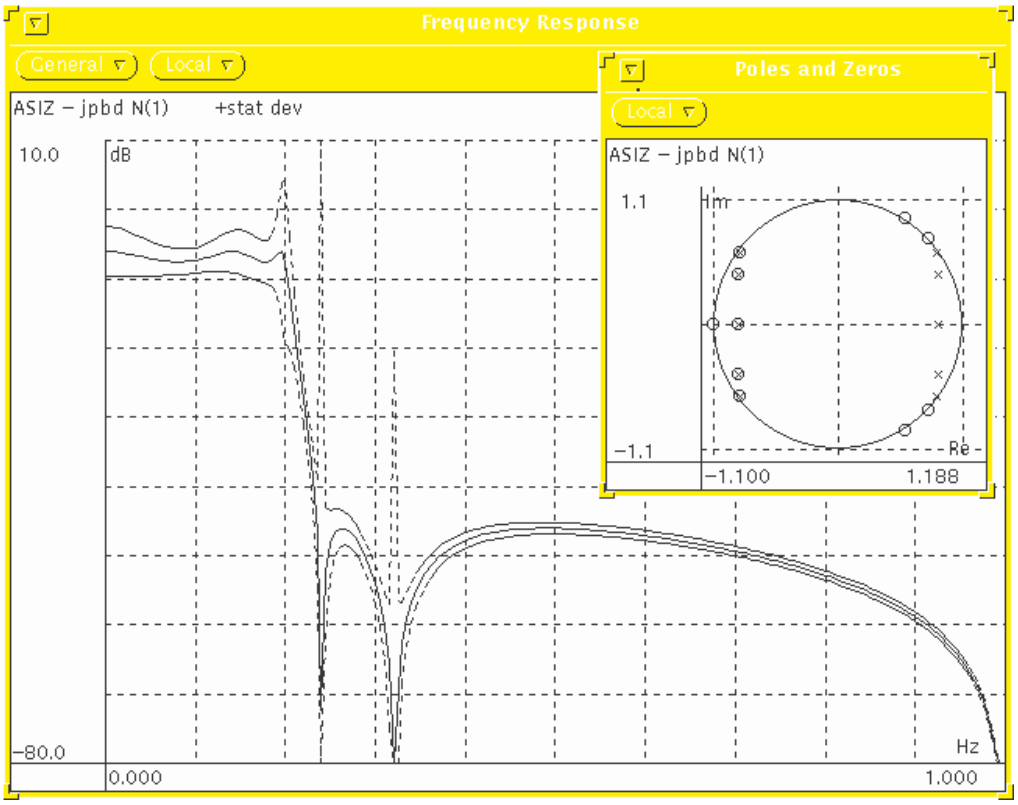
The ASIZ program: Developed at the Federal University of Rio de Janeiro, the ASIZ program analyses multi-phase circuits, computing:

- Transfer functions in *z*-transform.
- Poles and zeros.
- Frequency responses and output spectrum.
- Transient responses.
- Frequency-domain sensitivities.
- Effect of parasitic elements.
- Effect of component tolerances.

The circuit is assumed as a linear time-invariant Gm-C circuit, that reaches the steady state in a time negligible when compared with the duration of a phase. This allows the application of a nodal analysis method that is a generalization of a method used for ideal switched-capacitor circuits.

In the next page are screen images from the DOS and Sun versions. The Windows version is similar.


Frequency Response
Fr: 450.2806 Ga: -1.4667 Ph: -81.9989
10.0dB,deg
Messages
Partial numerator N(1,2,2):
0.000000E+0000 z^(0
2.960050E-0002 z^(1
-4.507811E-0002 z^(2
3.050303E-0002 z^(3
3.050303E-0002 z^(4
-4.507811E-0002 z^(5
2.960050E-0002 z^(6
Denominator:
0.000000E+0000 z^(0
-6.085462E-0001 z^(1
2.984896E+0000 z^(2
-6.197873E+0000 z^(3
6.812171E+0000 z^(4
-3.875623E+0000 z^(5
1.000000E+0000 z^(6
Poles and Zeros
Zero 5: 0.87562 0.48300j
1.1Im
-1.1
Re
-1.100
1.441
3.0Vi,Vo(V)
-1.0
t(s)
0.000
0.002
Hz
8000.000


Frequency Response
General
Local
ASIZ – jpbd N(1) +stat dev
10.0
dB
-80.0
Hz
0.000
1.000
Poles and Zeros
Local
ASIZ – jpbd N(1)
1.1
Im
-1.1
Re
-1.100
1.188

Other analysis algorithms/programs applied to SI circuits

- The WATSNAP program, developed at the University of Waterloo, can analyze SI circuits in small-signal operation, treating them as linear periodically switched linear circuits, computing:
  - Frequency response
  - Transient response
  - Natural frequencies
  - Sensitivities
- The algorithm used takes into account effects of incomplete stabilization.
- Some other programs developed for the analysis of non-ideal switched-capacitor circuits can also be used in the analysis of SI circuits, and compute other characteristics, as for example, noise (SCALP2), or approximate transfer functions in z-transform obtained by oversampling the continuous-time frequency responses obtained
- Classical time-domain simulation (SPICE) can be used for the analysis of nonlinear effects, provided that the transistor models are accurate, inclusive in the modeling of non-linear capacitances.

Last update: 10/8/2015