EXPERIMENTAL BIPOLAR REALIZATION OF A SWITCHED-CURRENT FILTER

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ABSTRACT

The paper describes techniques for the experimental construction of switched-current circuits, using discrete bipolar transistors and passive components. The techniques developed are useful as a mean for "breadboard" testing of new structures and examination of effects of nonidealities. The bipolar design can be also used in fully integrated BiCMOS realizations, with some the ideas having also applications in CMOS realizations, leading to wider dynamic range and better linearity.

1. INTRODUCTION

The "breadboard" construction of switched-current (SI) structures is problematic, due to the need of MOS transistors with different W/L ratios. Here we describe an approach for the experimental study of SI filters, using readily available discrete bipolar transistors, resistors, and capacitors. The structures developed with this purpose are in themselves interesting, because some of the ideas used are also applicable to integrated CMOS realizations, resulting in greater dynamic range and better linearity, and to possible BiCMOS realizations.

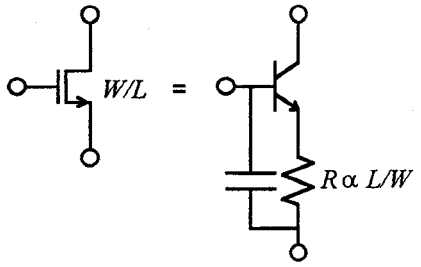

Fig. 1. Basic bipolar equivalent of a MOS transistor.

The basic idea is the substitution of MOS transistors in an SI structure, where current mirror gains are controlled by the W/L ratios of the transistors, by bipolar transistors with sufficiently large resistors connected in series with the emitters. The mirror gains are then controlled by resistance ratios (fig. 1). The switches are implemented by usual 4066 CMOS analog switches. The input capacitance of the MOS transistor, essential to the operation of SI circuits, is simulated by an added capacitor. The base-emitter junction capacitances of the transistors could be used, with a sufficiently high switching frequency, but the clock feedthrough effects caused by the analog switches would be rather high.

In the following sections, we describe the design and the experimental results with a "first-generation" bilinear SI filter, and then extend the developed ideas to designs for "second-generation" and "component-simulation" structures.

2. DESIGN OF A "FIRST-GENERATION" FILTER

The first design problem, that is insignificant in CMOS realizations, but not in bipolar realizations, is the discharge of the memory capacitors by the base currents of the transistors. Darlington-connected transistors must be used for transistors that memorize currents to minimize this problem. It is not sufficient to use larger capacitors, because this would make too slow the stabilization of switched current mirrors, as the ones used in "first-generation" SI circuits (fig. 2). If single transistors were used, the ratio between the time constants of capacitor discharges by base currents and the time constants of capacitor charges by diode-connected transistors would be of the order of the *hfe* of the transistors. With Darlington pairs, the ratio increases to about hfe^2.

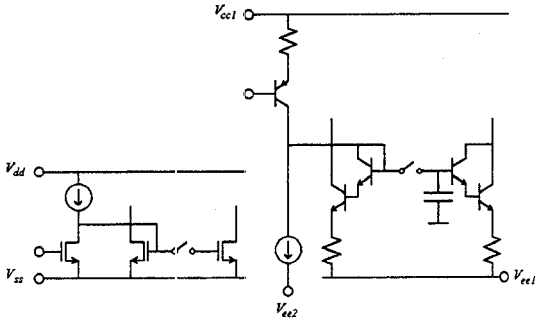

Fig. 2. Example of conversion from a CMOS SI "first generation" structure, showing the necessary changes.

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Another problem is that it is not practical to have diode-connected transistors driven from current sources made with transistors of the same kind (see fig. 2). Because of the emitter resistors (assumed connected to the same supply voltage), a circuit like this would allow only about 0.6 V of voltage excursion over the emitter resistors (even with Darlington transistors), before a transistor leaves the active region, with its base-collector junction forward-biased, and the corresponding current excursion would be very small. The solution is to stabilish a "connection rule" saying that diode-connected NPN(PNP) transistors must be driven from PNP(NPN) current sources.

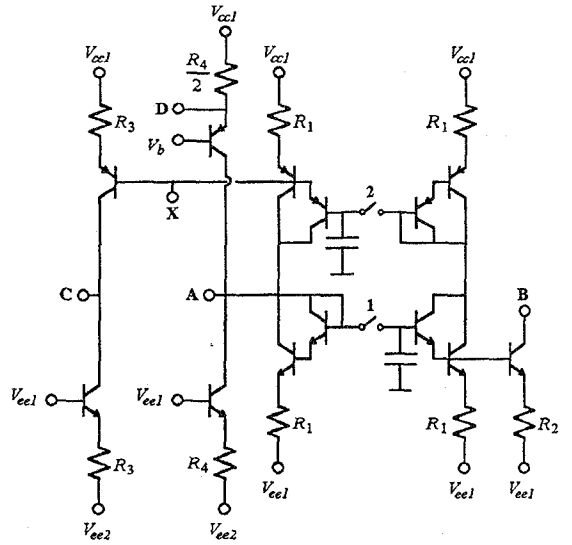

Fig. 3. First-generation integrator, with inverting ("B") and noninverting ("C") outputs, and two possible equivalent inputs ("A", "D"). Point "X" is used in the output circuit (fig. 4).

Fig. 3 shows a complete converted "first-generation" SI integrator, where some of the design details mentioned above can be observed:

The loop of two current sample/hold cells is made with switched mirrors of NPN and PNP transistors. This satisfies the rule about connections of current sources to diode-connected transistors, and also eliminates the need of biasing current sources for the integrator transistors. The no-signal current is stabilized indirectly by the current sources associated with the output current copies.

The Point "A" is the input for the integrator. Most first-generation SI filters can be made from integrators having input at this point only. The interconnection rule requires that any current entering point "A" must come from a PNP transistor. The two possible integrator outputs are points "B" and "C". The output "C" can be connected directly to an input "A" of a similar integrator. The output "B" must be connected to a point like "D" to pass the signal correctly to another integrator. All the integrators are built with the "A" and "D" inputs, that act equivalently, with point "A" being used for outputs coming from "C" outputs, and point "D" being used for inputs coming from "B" outputs.

The transistors with bases connected to V_{ee2} are fixed bias current sources. With this connection, and $V_{ee2}<V_{ee1}$, the current sources work correctly, without violating the connection rule, because the points "A" and "C" are always at voltages higher than V_{ee1}.

The voltage V_b is chosen to make $V_{cc1}-V_b = V_{ee1}-V_{ee2}$. In this way, R_4 is equal to the parallel connection of all the R_2 resistors of the "B" outputs connected to input "D", and the two R_3 resistors of each output "C" are equal. The ratios R_3/R_1 and R_2/R_1 control the output gains of the integrator. A few "C" and "B" outputs can be added to each integrator without much degradation due to discharge of the memory capacitors.

Note that actually just one fixed current source is required for each integrator. The current sources associated to the "C" outputs could be incorporated to the current sources associated to the "D" inputs by simply adding all the R_3 resistors in parallel with the R_4 resistors (This was not done in the experimental filter).

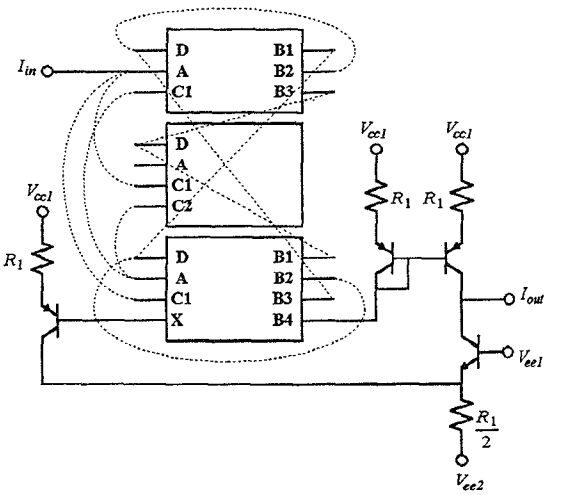

Fig. 4. Interconnection of 3 integrators, building a 3rd-order bilinear elliptic filter.

To test the viability of the construction method, a 3rd-order bilinear elliptic low-pass filter (1 dB passband ripple, 40 dB stopband attenuation) was built with three of the integrators shown in fig. 3, in a configuration simulating an LC doubly terminated passive prototype, of a type similar to the ones described in [1], page 245. A "first-generation" structure was chosen due to the simpler two-phases nonoverlapping clocking system, even with the resulting filter being suboptimal in sensitivity. The complete structure is represented in fig. 4. The filter was designed for 20:1 ratio between the switching frequency and the passband border frequency. It was powered with ±6 V

main supplies (V_{cc1}, V_{ee1}), V_b=+4 V, and V_{ee2}=–8 V. The resistors R_1 were set to 22 kΩ, resulting in no-signal integrator currents of about 65 μA. The total current consumption of the filter was of less than 1 mA. The nominal switching frequency was designed to be of 5 kHz, with 1 nF hold capacitors being used, what results in approximately 5 time constants (with R_1) for stabilization in each of the two phases. The input current was generated by a 3080 OTA, and the output was taken as the voltage over a grounded load resistor.

3. EXPERIMENTAL RESULTS

The filter operated correctly, requiring only a small offset adjust (by changing the emitter resistor of a bias current source) to optimize the dynamic range of the central section (the most sensitive to DC offsets). A small Q enhancement was observed at the passband border, attributable to component mismatches, since first-generation circuits are of relatively high sensitivity.

It was observed that the switching frequency could be varied from about 500 Hz to 10 kHz without significant degradation of the filter performance. At the higher end, the first noticeable effect of the incomplete stabilization of the capacitor voltages was a trend for the stabilization of the filter operating frequency, that ceased to be proportional to the switching frequency. This effect was followed by Q decreasing and soon by the generation of offset voltages and nonlinearities, possibly due to increased clock feedthrough. At the lower end, offset DC signals generated by the irregular discharge of the hold capacitors through the base currents (different, because the transistors were not matched) were observed to be the dominant error.

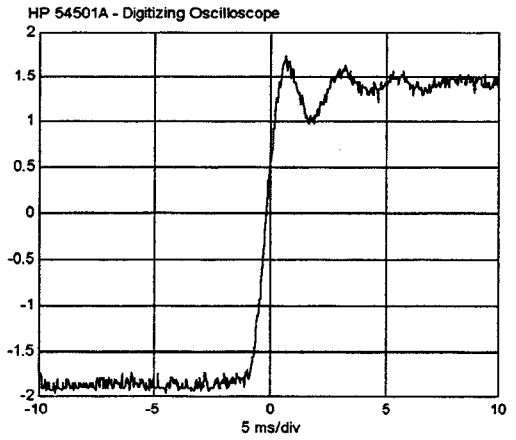

Fig. 5. Transient response of a step transition, used to evaluate the filter performance.

These results were obtained by the application to the filter of a low-frequency square wave, and the observation of the resulting transition transients (fig. 5), while the switching frequency was varied. Fig. 6 shows the ideal transient response for that filter, computed by the ASIZ program [1], scaled to fit scales similar to those in fig. 5. The switching frequency is 9 kHz.

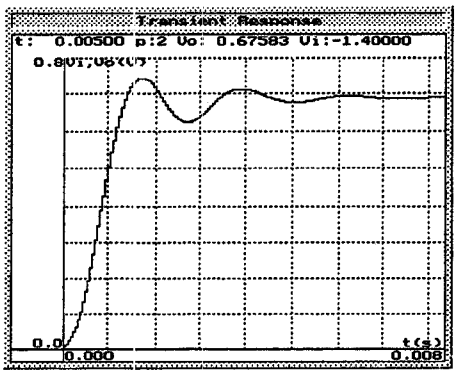

Fig. 6. Ideal step response.

Fig. 7 plots the apparent frequency of the oscillating transient (due to the two complex poles of the filter), relative to the switching frequency, where the stabilization of the filter operating frequency at the high end can be observed. In all the measured range shown, offset generation and Q changes were negligible.

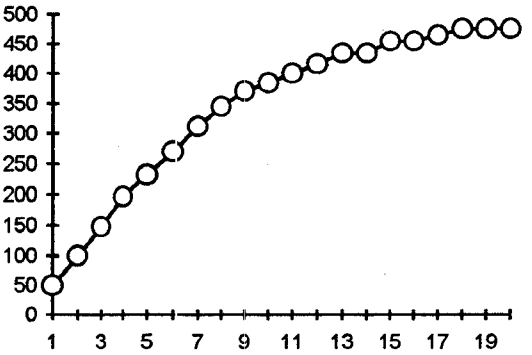

Fig. 7. Measured oscillating frequency of the transient response (Hz) versus switching frequency (kHz) in the test filter.

4. "SECOND-GENERATION" FILTERS

"Second-generation" SI structures [1] can be built using the same ideas. There is some complication, however, due to the two different inputs that can be required. Fig. 8 illustrates a possible implementation of an integrator.

The two S/H cells are realized by two NPN Darlington pairs. As the connection rule forbids the diode connection of one of the pairs when one of the switches (1,2) closes, a folded cascode structure is required to make the connections. R_7 controls the current drained by the folded cascode, that can be a fraction of the nominal current in the S/H cells. Outputs "B" and "C", with gains R_1/R_2 and R_1/R_3, can be added to each side of the S/H pair. "A" is the normal current input, and "D" a direct input that can

be used in the simulation of passive ladder networks [2]. With V_{cc1}-V_b = V_{ee1}-V_{ee2}, R_6 = R_1/2//R_7//(all the R_2 and R_3 from outputs connected to "D"), and R_4=(parallel connection of all the R_2 and R_3 of outputs connected to "A"). More precision can be obtained by replacing R_4 and R_6 by current sources. The correct operation requires four clock phases (1,2,1', 2') [2].

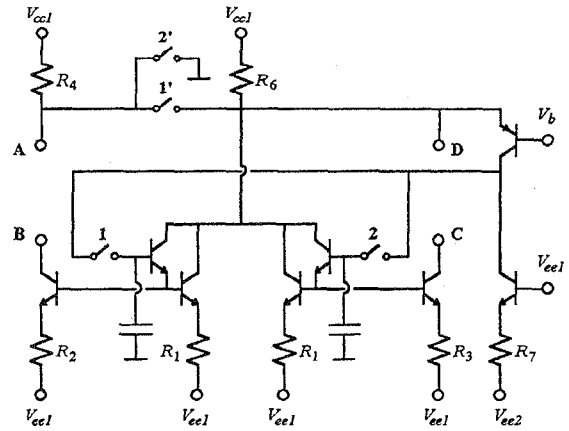

Fig. 8. A "second-generation" integrator.

5. "COMPONENT-SIMULATION" STRUCTURES

"Component-simulation" SI structures [3] are based on the simulation of a Gm-C equivalent of a passive prototype, with the capacitances and transconductances realized by SI circuits that correspond to discretized transcapacitances and transconductances. These structures operate with doubled sampling rate with a two-phases clock system, and can be almost as insensitive to component mismatches as "second-generation" structures.

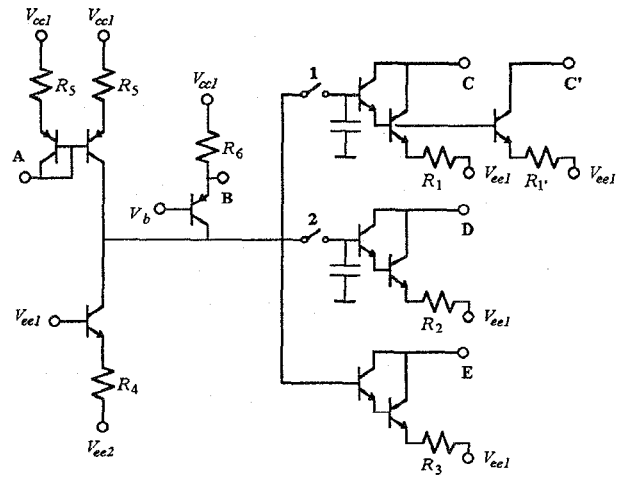

Fig. 9. A general node for component-simulation structures.

The bipolar realization of the general building block, a "node", is shown in fig. 9. There are two possible inputs (noninverting and inverting), "A" and "B", that can be connected to outputs "C", "D", and "E". Multiple outputs are added as exemplified by "C'". A folded cascode structure allows the connection of outputs to the inverting input without violation of the connection rule. With the voltage supplies as in the other circuits, R_5 = (parallel connection of all the R_1, R_2, and R_3 of the outputs connected to "A"), R_6 = R_7//(parallel connection of all the R_1, R_2, and R_3 of the outputs connected to "B"), and R_4=R_5//R_6. R_7 (part of R_6) controls the current in the folded cascode transistor.

6. CONCLUSION

The viability of the experimental construction of SI filters with discrete components, using bipolar transistors as active devices, was demonstrated. The resulting structures may be not very practical for actual applications, but are useful for studies about structures for SI filters, allowing the experimental observation of some effects, mainly of imperfections, that may be not easy to observe by simulation or in integrated CMOS realizations.

The changes in conventional CMOS structures required by the bipolar design are also applicable to CMOS structures, possibly resulting in higher dynamic range and linearity, and smaller losses, because the transistor's operating points are kept more inside the saturation region.

BiCMOS fully integrated realizations, with the current-mirror gains controlled by emitter area ratios instead of resistors, and the switches implemented with MOS transistors, appear to be viable. The discharge of the storage capacitances through the transistor bases appears to have as main effect only some DC offset generation. In a BiCMOS process, the Darlington transistors can be implemented with a MOS transistor at the first transistor, eliminating this problem. The higher transconductances obtainable from bipolar devices may reduce the stabilization time of the SI circuits, allowing the construction of faster filters.

REFERENCES

[1] C. Toumazou, J. B. Hughes, and N. C. Battersby, eds,. "*Switched-Currents, an Analogue Technique for Digital Technology*," Peter Peregrinus/IEE, London, UK, 1993.

[2] A. C. M. de Queiroz and P. R. M. Pinheiro, "Bilinear switched-current ladder filters using Euler integrators," *IEEE Transactions on Circuits and Systems-II*, Vol. 43, No. 1, pp. 66-70, January 1996.

[3] J. Schechtman, A. C. M. de Queiroz, and L. P. Calôba, "A practical implementation scheme for Component Simulation SI filters," *Proc. 38th MWSCAS*, Rio de Janeiro, Brazil, pp. 174-177, August 1995.